

**AHC/AHCT Logic**  
**Advanced High-Speed CMOS**

*Data Book*

**1996**

***Advanced System Logic Products***

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# **AHC/AHCT Logic Advanced High-Speed CMOS Data Book**

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## INTRODUCTION

The Advanced High-speed CMOS (AHC) logic family provides a natural migration for HCMOS users who need more speed for low-power, low-noise, and low-drive applications. The AHC logic family consists of basic gates, medium-scale integrated circuits, and octal functions fabricated using the EPIC1-S process that produces high performance at low cost.

Performance characteristics of the AHC family are:

- Speed – With typical propagation delays of 5.2 ns (octals), which is about three times faster than HC devices, AHC devices are the quick and quiet solution for higher-speed operation.
- Low noise – The AHC family allows designers to combine the low-noise characteristics of HCMOS devices with today's performance levels without the overshoot/undershoot problems typical of higher-drive devices usually required to get AHC speeds.
- Low power – The AHC family, by using CMOS technology, exhibits low power consumption (40- $\mu$ A maximum static current, half that of HCMOS).
- Drive – Output drive current is  $\pm 8$  mA at 5-V  $V_{CC}$  and  $\pm 4$  mA at 3.3-V  $V_{CC}$ .
- Packaging – AHC devices are available in D and DW (SOIC), DB (SSOP), N (PDIP), and PW (TSSOP) packages. Selected AHC devices are available in military versions (SN54AHCxx).

Using Texas Instruments (TI) products offers several business advantages:

- Competitive advantage – AHC and VHC devices have equivalent specifications; therefore, AHC devices are "drop in" replaceable. With TI's production capacity, delivery performance, and competitive prices, AHC devices are among the most economical, easy-to-use, and easy-to-get logic products.
- Alternate source – TI has arrangements for one or more alternate sources for AHC devices.

For more information on these and other products, including availability dates, pricing, and final timing specifications, please contact your local Texas Instruments representative, authorized distributor, call the Advanced System Logic hotline at 903-868-5202, or visit the TI home page at <http://www.ti.com>.

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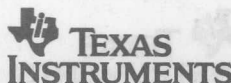
## INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

### operating conditions and characteristics (in sequence by letter symbols)

<b>C<sub>i</sub></b>	<b>Input capacitance</b> The internal capacitance at an input of the device
<b>C<sub>o</sub></b>	<b>Output capacitance</b> The internal capacitance at an output of the device
<b>C<sub>pd</sub></b>	<b>Power dissipation capacitance</b> Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$
<b>f<sub>max</sub></b>	<b>Maximum clock frequency</b> The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification
<b>I<sub>CC</sub></b>	<b>Supply current</b> The current into* the V <sub>CC</sub> supply terminal of an integrated circuit
<b>ΔI<sub>CC</sub></b>	<b>Supply current change</b> The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V <sub>CC</sub>
<b>I<sub>CEX</sub></b>	<b>Output high leakage current</b> The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition V <sub>O</sub> = 5.5 V
<b>I<sub>I(hold)</sub></b>	<b>Input hold current</b> Input current that holds the input at the previous state when the driving device goes to a high-impedance state
<b>I<sub>IH</sub></b>	<b>High-level input current</b> The current into* an input when a high-level voltage is applied to that input
<b>I<sub>IL</sub></b>	<b>Low-level input current</b> The current into* an input when a low-level voltage is applied to that input
<b>I<sub>off</sub></b>	<b>Input/output power-off leakage current</b> The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and V <sub>CC</sub> = 0 V
<b>I<sub>OH</sub></b>	<b>High-level output current</b> The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.
<b>I<sub>OL</sub></b>	<b>Low-level output current</b> The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

\*Current out of a terminal is given as a negative value.



## GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS

<b>I<sub>oz</sub></b>	<b>Off-state (high-impedance-state) output current (of a 3-state output)</b> The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output.
<b>t<sub>a</sub></b>	<b>Access time</b> The time interval between the application of a specified input pulse and the availability of valid signals at an output
<b>t<sub>c</sub></b>	<b>Clock cycle time</b> Clock cycle time is $1/f_{\text{max}}$ .
<b>t<sub>dis</sub></b>	<b>Disable time (of a 3-state or open-collector output)</b> The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state  NOTE: For 3-state outputs, $t_{\text{dis}} = t_{\text{PHZ}}$ or $t_{\text{PLZ}}$ . Open-collector outputs will change only if they are low at the time of disabling, so $t_{\text{dis}} = t_{\text{PLH}}$ .
<b>t<sub>en</sub></b>	<b>Enable time (of a 3-state or open-collector output)</b> The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low)  NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{\text{OE}}$ ). For 3-state outputs, $t_{\text{en}} = t_{\text{PZH}}$ or $t_{\text{PZL}}$ . Open-collector outputs will change only if they are responding to data that would cause the output to go low, so $t_{\text{en}} = t_{\text{PHL}}$ .
<b>t<sub>h</sub></b>	<b>Hold time</b> The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal  NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected. 2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.
<b>t<sub>pd</sub></b>	<b>Propagation delay time</b> The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ( $t_{\text{pd}} = t_{\text{PHL}}$ or $t_{\text{PLH}}$ )
<b>t<sub>PHL</sub></b>	<b>Propagation delay time, high-to-low level output</b> The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level
<b>t<sub>PHZ</sub></b>	<b>Disable time (of a 3-state output) from high level</b> The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state
<b>t<sub>PLH</sub></b>	<b>Propagation delay time, low-to-high level output</b> The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level



\*Current out of a terminal is given as a negative value.

## GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS



<b>tpLZ</b>	<b>Disable time (of a 3-state output) from low level</b> The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state
<b>tpZH</b>	<b>Enable time (of a 3-state output) to high level</b> The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level
<b>tpZL</b>	<b>Enable time (of a 3-state output) to low level</b> The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level
<b>t<sub>su</sub></b>	<b>Setup time</b> The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal  NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed. 2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.
<b>t<sub>w</sub></b>	<b>Pulse duration (width)</b> The time interval between specified reference points on the leading and trailing edges of the pulse waveform
<b>V<sub>IH</sub></b>	<b>High-level input voltage</b> An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables  NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.
<b>V<sub>IL</sub></b>	<b>Low-level input voltage</b> An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables  NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.
<b>V<sub>OH</sub></b>	<b>High-level output voltage</b> The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output
<b>V<sub>OL</sub></b>	<b>Low-level output voltage</b> The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output
<b>V<sub>IT+</sub></b>	<b>Positive-going input threshold level</b> The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V <sub>IT-</sub>
<b>V<sub>IT-</sub></b>	<b>Negative-going input threshold level</b> The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V <sub>IT+</sub>

## EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . . h	=	the level of steady-state inputs A through H, respectively
Q <sub>0</sub>	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q <sub>0</sub> or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q <sub>n</sub>	=	level of Q before the most recent active transition indicated by ↓ or ↑
	=	one high-level pulse
	=	one low-level pulse
Toggle	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q<sub>0</sub>, or  $\overline{Q}_0$ ), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse,  or , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)





Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
	S <sub>1</sub>	S <sub>0</sub>		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	H	H	H	H	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>
H	L	H	↑	X	L	L	L	L	L	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>
H	H	L	↑	H	X	X	X	X	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	H
H	H	L	↑	L	X	X	X	X	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	L
H	L	L	X	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S<sub>1</sub> and S<sub>0</sub> are both high then, without regard to the serial input, the data entered at A will be at output Q<sub>A</sub>, data entered at B will be at Q<sub>B</sub>, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q<sub>A</sub> is now at Q<sub>B</sub>, the previous levels of Q<sub>B</sub> and Q<sub>C</sub> are now at Q<sub>C</sub> and Q<sub>D</sub>, respectively, and the data previously at Q<sub>D</sub> is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S<sub>1</sub> is low and S<sub>0</sub> is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q<sub>B</sub> is now at Q<sub>A</sub>, the previous levels of Q<sub>C</sub> and Q<sub>D</sub> are now at Q<sub>B</sub> and Q<sub>C</sub>, respectively, and the data previously at Q<sub>A</sub> is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S<sub>1</sub> is high and S<sub>0</sub> is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

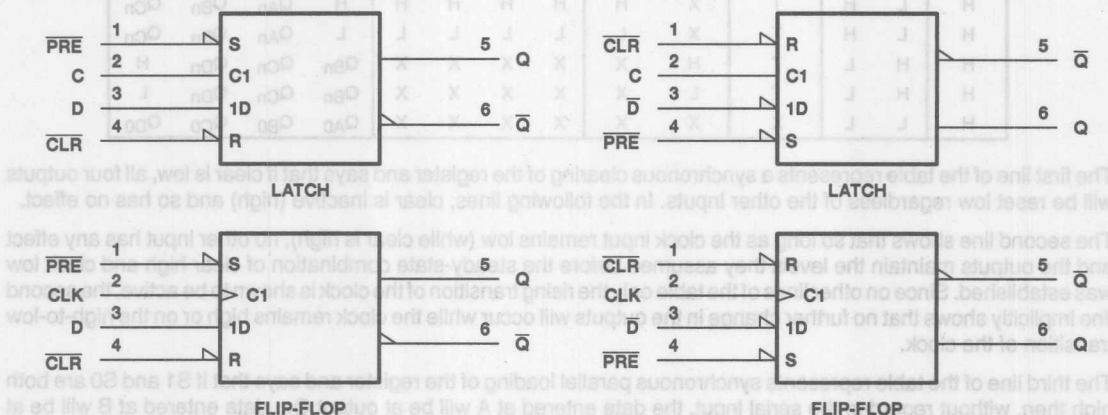
The function table functional tests do not reflect all possible combinations or sequential modes.

## D FLIP-FLOP AND LATCH SIGNAL CONVENTIONS

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called  $\bar{Q}$ . An input that causes a Q output to go high or a  $\bar{Q}$  output to go low is called preset (PRE). An input that causes a  $\bar{Q}$  output to go high or a Q output to go low is called clear ( $\bar{CLR}$ ). Bars are used over these pin names ( $\bar{PRE}$  and  $\bar{CLR}$ ) if they are active low.

The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits  $\bar{D}$  and Q.

In some applications, it may be advantageous to redesignate the data input from D to  $\bar{D}$  or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and  $\bar{Q}$  exchange names, the preset and clear pins also exchange names. The polarity indicators ( $\triangle$ ) on  $\bar{PRE}$  and  $\bar{CLR}$  remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or  $\bar{D}$ ), Q, and  $\bar{Q}$ . Pin 5 (Q or  $\bar{Q}$ ) is still in phase with the data input (D or  $\bar{D}$ ); their active levels change together.

## THERMAL INFORMATION

In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures. In general, the junction temperature for any device can be calculated using the following equation:

$$T_J = R_{\theta JA} \times P_T + T_A$$

Where:

- $T_J$  = virtual junction temperature
- $R_{\theta JA}$  = thermal resistance, junction to free air
- $P_T$  = total power dissipation of the device
- $T_A$  = free-air temperature

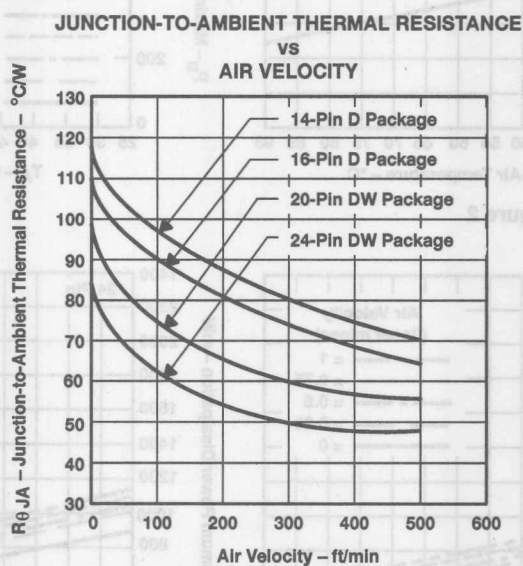


Figure 1

Derating curves for 210-mil shrink small-outline package are shown in Figures 2 through 5.



# THERMAL INFORMATION

## DERATING CURVES FOR 210-MIL SHRINK SMALL-OUTLINE PACKAGE (DB)

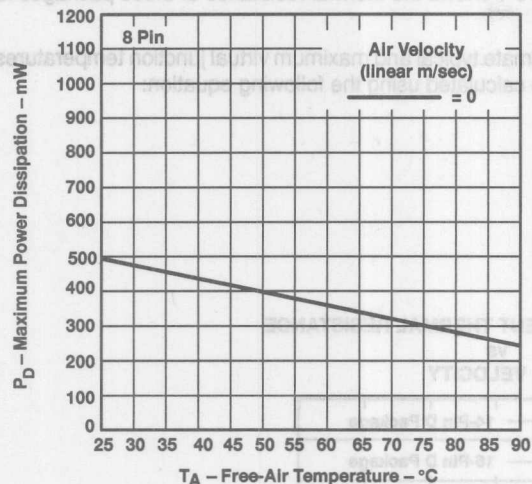


Figure 2

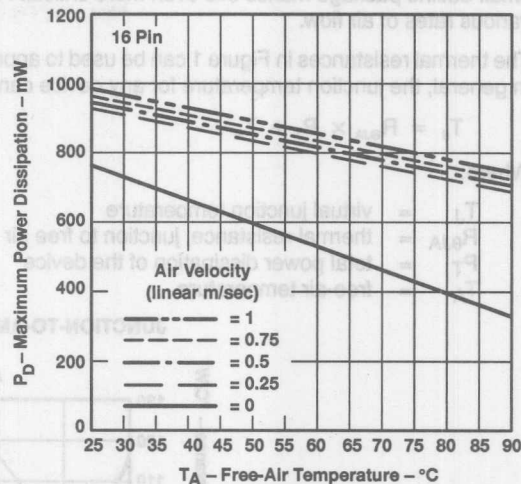


Figure 3

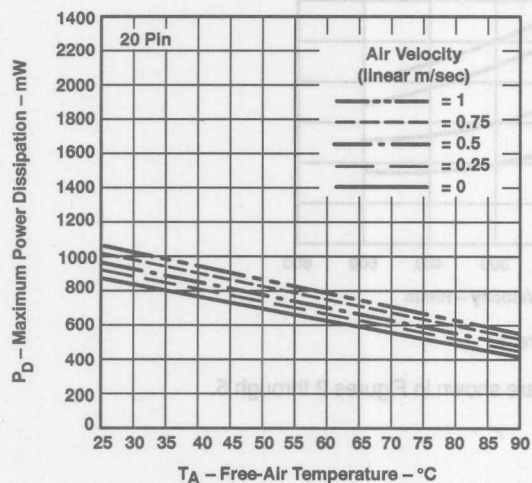


Figure 4

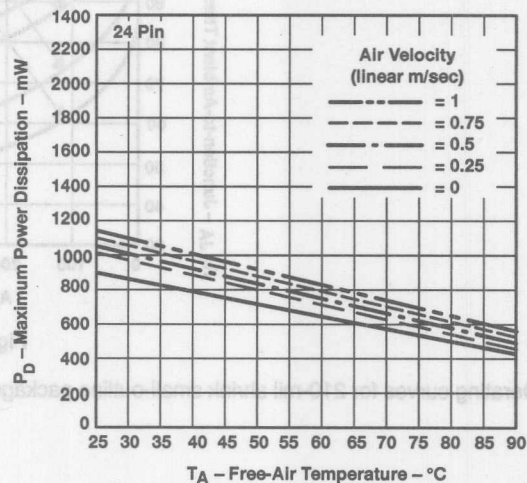


Figure 5

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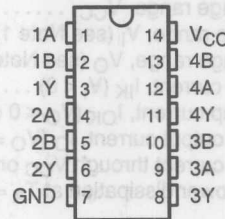
# SN74AHC00

## QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS227 – OCTOBER 1995

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



### description

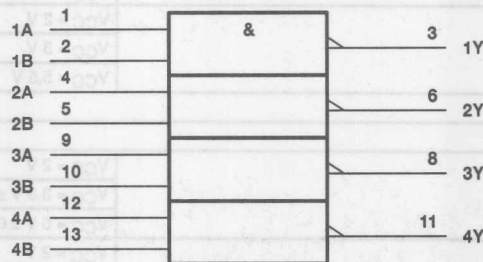
The SN74AHC00 performs the Boolean functions  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

The SN74AHC00 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram, each gate (positive logic)



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PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN74AHC00

## QUADRUPLE 2-INPUT POSITIVE-NAND GATE

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W

Storage temperature range,  $T_{stg}$  ..... -65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 3$ V	2.1	
		$V_{CC} = 5.5$ V	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 3$ V	0.9	
		$V_{CC} = 5.5$ V	1.65	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	-50	μA
		$V_{CC} = 3.3 \pm 0.3$ V	-4	mA
		$V_{CC} = 5 \pm 0.5$ V	-8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 3.3 \pm 0.3$ V	4	mA
		$V_{CC} = 5 \pm 0.5$ V	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \pm 0.3$ V	100	ns/V
		$V_{CC} = 5 \pm 0.5$ V	20	
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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# **SN74AHC00** **QUADRUPLE 2-INPUT POSITIVE-NAND GATE**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
I <sub>I</sub>	A or B inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		±0.1		±1	µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		2		20	µA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10	10	pF

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF		5.5	7.9	1	9.5	ns
t <sub>PHL</sub>					5.5	7.9	1	9.5	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF		8	11.4	1	13	ns
t <sub>PHL</sub>					8	11.4	1	13	

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF		3.7	5.5	1	6.5	ns
t <sub>PHL</sub>					3.7	5.5	1	6.5	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF		5.2	7.5	1	8.5	ns
t <sub>PHL</sub>					5.2	7.5	1	8.5	

noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 4)

PARAMETER	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub> Quiet output, maximum dynamic V <sub>OL</sub>		0.3	0.8	V
V <sub>OL(V)</sub> Quiet output, minimum dynamic V <sub>OL</sub>		-0.3	-0.8	V
V <sub>OH(V)</sub> Quiet output, minimum dynamic V <sub>OH</sub>		4.6		V
V <sub>IH(D)</sub> High-level dynamic input voltage		3.5		V
V <sub>IL(D)</sub> Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.



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# SN74AHC00

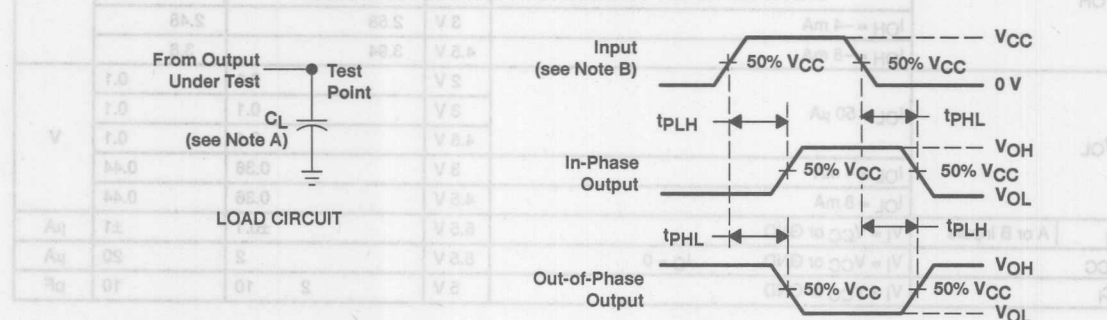
## QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS227 - OCTOBER 1995

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	9.5	pF

### PARAMETER MEASUREMENT INFORMATION



### VOLTAGE WAVEFORMS DELAY TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$	
				MIN	MAX
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$	3.7	8.5
$t_{PHL}$	A or B	Y	$C_L = 15\text{ pF}$	3.7	8.5
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$	3.7	8.5
$t_{PHL}$	A or B	Y	$C_L = 50\text{ pF}$	3.7	8.5

PARAMETER	UNIT
$V_{OH}$ High-level output voltage	V
$V_{OL}$ Low-level output voltage	V
$V_{IH}$ High-level input voltage	V
$V_{IL}$ Low-level input voltage	V



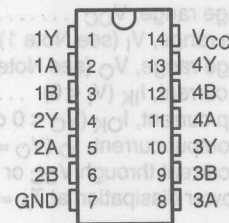
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# SN74AHC02 QUADRUPLE 2-INPUT POSITIVE-NOR GATE

SCLS254A – DECEMBER 1995 – REVISED FEBRUARY 1996

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

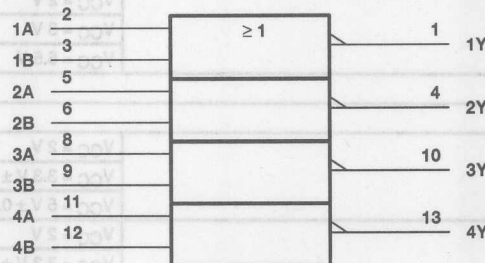
This device contains four independent 2-input NOR gates that perform the Boolean functions  $Y = \bar{A} \cdot \bar{B}$  or  $Y = A + B$  in positive logic.

The SN74AHC02 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each gate)

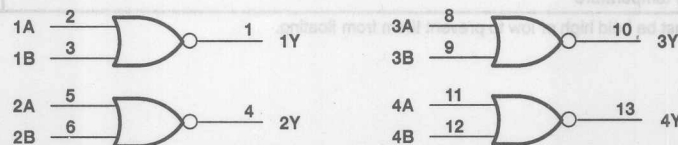
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

## logic symbol



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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PRODUCT PREVIEW



SN74AHC02  
QUADRUPLE 2-INPUT POSITIVE-NOR GATE

SCLS254A – DECEMBER 1995 – REVISED FEBRUARY 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 3$ V	2.1	
		$V_{CC} = 5.5$ V	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 3$ V	0.9	
		$V_{CC} = 5.5$ V	1.65	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	–50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	–4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	–8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	100	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	20	
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

# SN74AHC02

## QUADRUPLE 2-INPUT POSITIVE-NOR GATE

SCLS254A – DECEMBER 1995 – REVISED FEBRUARY 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
		4.5 V			0.36		0.44	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10		10	pF

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF		5.6	7.9	1	9.5	ns
t <sub>PHL</sub>					5.6	7.9	1	9.5	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF		8.1	11.4	1	13	ns
t <sub>PHL</sub>					8.1	11.4	1	13	

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF		3.6	5.5	1	6.5	ns
t <sub>PHL</sub>					3.6	5.5	1	6.5	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF		5.1	7.5	1	8.5	ns
t <sub>PHL</sub>					5.1	7.5	1	8.5	

noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>			0.8	V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>			-0.8	V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>				V
V <sub>IH(D)</sub>	High-level dynamic input voltage	3.5			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.



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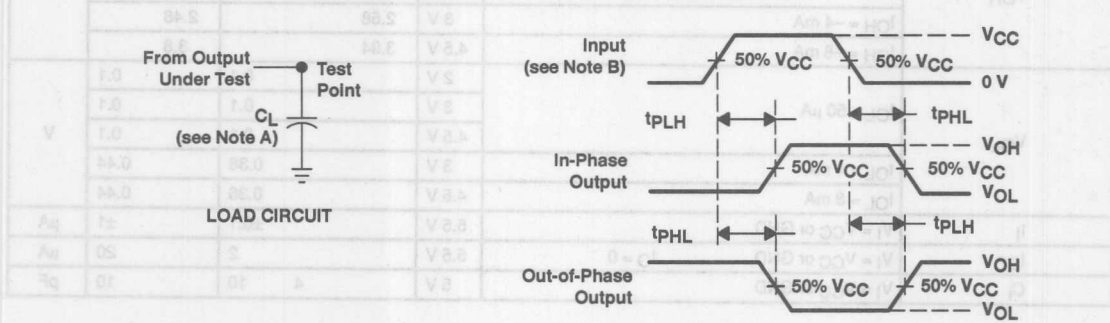
SN74AHC02  
QUADRUPLE 2-INPUT POSITIVE-NOR GATE

SCLS254A – DECEMBER 1995 – REVISED FEBRUARY 1996

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per gate	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	15	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .
  - C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			UNIT
				MIN	TYP	MAX	
$t_{PLH}$	A to B	Y	$C_L = 15\text{ pF}$	0.8	0.8	1.0	ns
$t_{PHL}$	A to B	Y	$C_L = 15\text{ pF}$	0.8	0.8	1.0	ns
$t_{PLH}$	A to B	Y	$C_L = 50\text{ pF}$	0.8	0.8	1.0	ns
$t_{PHL}$	A to B	Y	$C_L = 50\text{ pF}$	0.8	0.8	1.0	ns

PARAMETER				UNIT
MIN	TYP	MAX	MAX	
$V_{OH}$			5.0	V
$V_{OL}$			0.5	V
$V_{IH}$			5.0	V
$V_{IL}$			0.5	V

NOTE 4: Characteristics are determined during product characterization and entered by design for surface-mount packages only.



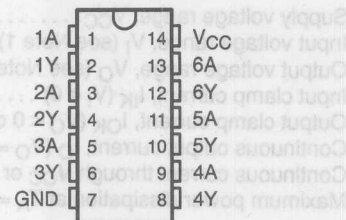
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# SN74AHC04 HEX INVERTER

SCLS231B – OCTOBER 1995 – REVISED JANUARY 1996

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

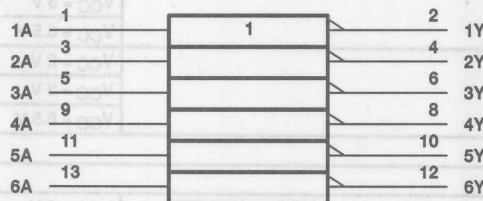
The SN74AHC04 contains six independent inverters. The device performs the Boolean function  $Y = \bar{A}$ .

The SN74AHC04 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# SN74AHC04 HEX INVERTER

SCLS231B – OCTOBER 1995 – REVISED JANUARY 1996

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 3$ V	2.1	
		$V_{CC} = 5.5$ V	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 3$ V	0.9	
		$V_{CC} = 5.5$ V	1.65	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	–50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	–4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	–8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	100	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	20	
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = – 50 µA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = – 4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = – 8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			± 0.1		± 1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF		5	7.1	1	8.5	ns
t <sub>PHL</sub>					5	7.1	1	8.5	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF		7.5	10.6	1	12	ns
t <sub>PHL</sub>					7.5	10.6	1	12	

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF		3.8	5.5	1	6.5	ns
t <sub>PHL</sub>					3.8	5.5	1	6.5	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF		5.3	7.5	1	8.5	ns
t <sub>PHL</sub>					5.3	7.5	1	8.5	

noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.4		V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		–0.4		V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>		4.8		V
V <sub>IH(D)</sub>	High-level dynamic input voltage	3.5			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

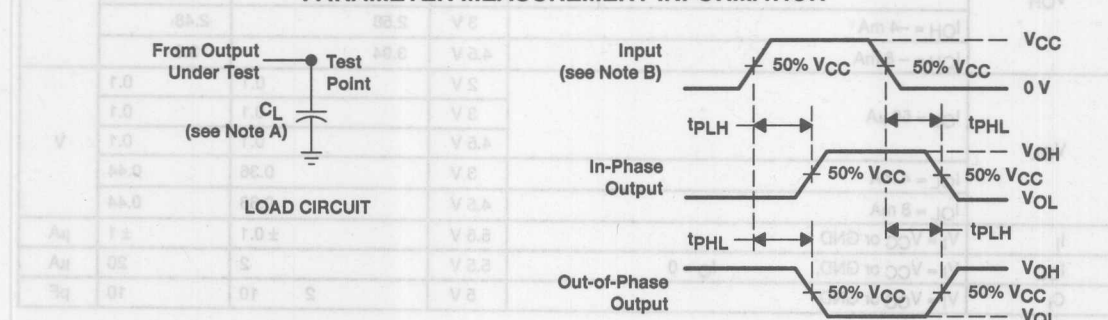
# SN74AHC04 HEX INVERTER

SCLS231B - OCTOBER 1995 - REVISED JANUARY 1996

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	12	pF

## PARAMETER MEASUREMENT INFORMATION



## VOLTAGE WAVEFORMS DELAY TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	TYP	MAX	UNIT
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$	0.5	0.5	1.0	ns
$t_{PHL}$	A	Y	$C_L = 50\text{ pF}$	0.5	0.5	1.0	ns

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OH}$ Output high voltage	4.5			V
$V_{OL}$ Output low voltage	0.5			V
$V_{IH}$ Input high voltage	4.5			V
$V_{IL}$ Input low voltage	0.5			V

NOTE 4: Characteristics are determined during production testing and are not guaranteed for all devices.



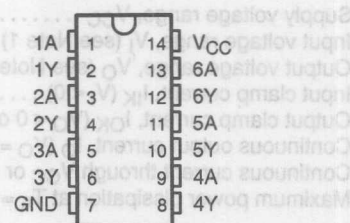
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# SN74AHCU04 HEX INVERTER

SCLS234 – OCTOBER 1995

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Unbuffered Outputs
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

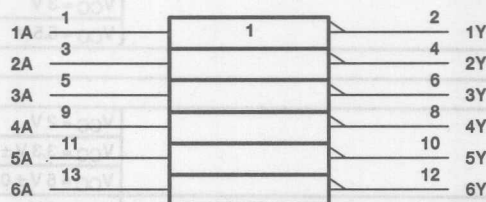
The SN74AHCU04 contains six independent inverters. The device performs the Boolean function  $Y = \bar{A}$ . Internal circuitry consists of single stage inverters that can be used in analog applications such as crystal oscillators.

The SN74AHCU04 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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SN74AHCU04  
HEX INVERTER

SCLS234 – OCTOBER 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W

Storage temperature range,  $T_{stg}$  ..... -65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.7	V
		$V_{CC} = 3$ V	2.4	
		$V_{CC} = 5.5$ V	4.4	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.3	V
		$V_{CC} = 3$ V	0.6	
		$V_{CC} = 5.5$ V	1.1	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	-50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	-4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	-8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	8	
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V	1.8	2		1.8		V
		3 V	2.7	3		2.7		
		4.5 V	4	4.5		4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V			0.2		0.2	V
		3 V			0.3		0.3	
		4.5 V			0.5		0.5	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	5	8.9		1	10.5	ns
t <sub>PHL</sub>				5	8.9		1	10.5	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	7.5	11.4		1	13	ns
t <sub>PHL</sub>				7.5	11.4		1	13	

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	3.5	5.5		1	6.5	ns
t <sub>PHL</sub>				3.5	5.5		1	6.5	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	5	7		1	8	ns
t <sub>PHL</sub>				5	7		1	8	

noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.5		V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		-0.5		V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>		4.3		V
V <sub>IH(D)</sub>	High-level dynamic input voltage	4			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			1	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

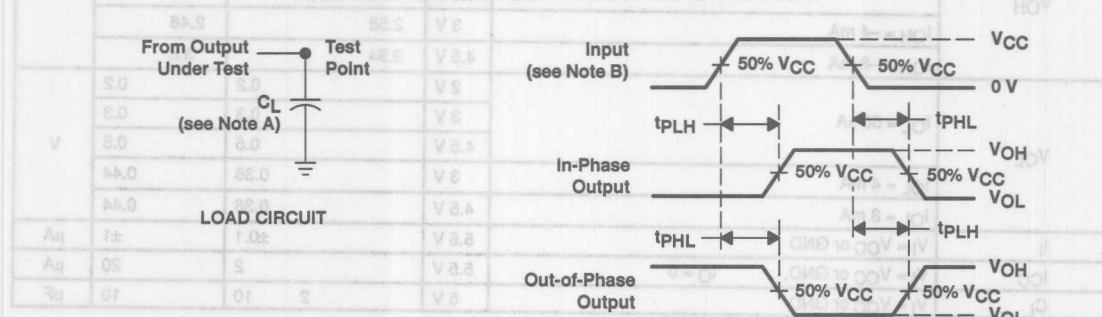
# SN74AHC04 HEX INVERTER

SCLS234 – OCTOBER 1995

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	7.3	pF

## PARAMETER MEASUREMENT INFORMATION



## VOLTAGE WAVEFORMS DELAY TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	MIN	TYP	MAX	UNIT
$t_{PLH}$	A	Y	$C_L = 10\text{ pF}$	0.5	0.5	1	ns
$t_{PHL}$	A	Y	$C_L = 10\text{ pF}$	0.5	0.5	1	ns

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OH}$ Quiet output, minimum dynamic $V_{OH}$	4.5			V
$V_{OL}$ Quiet output, maximum dynamic $V_{OL}$	0.5			V
$V_{IH}$ High-level dynamic input voltage	1			V
$V_{IL}$ Low-level dynamic input voltage	0.5			V

NOTE 4: Characteristics are determined during product characterization and should be used for customer-mount packages only.

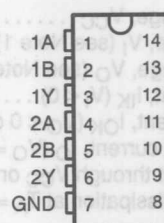


# SN74AHC08 QUADRUPL 2-INPUT POSITIVE-AND GATE

SCLS236 – OCTOBER 1995

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

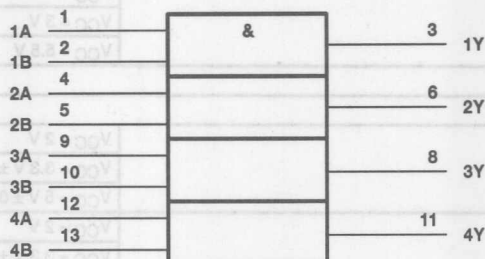
The SN74AHC08 is a quadruple 2-input positive-AND gate. The device performs the Boolean functions  $Y = A \cdot B$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

The SN74AHC08 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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SN74AHC08  
QUADRUPLE 2-INPUT POSITIVE-AND GATE

SCLS236 – OCTOBER 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W

Storage temperature range,  $T_{stg}$  –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 3$ V	2.1	
		$V_{CC} = 5.5$ V	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 3$ V	0.9	
		$V_{CC} = 5.5$ V	1.65	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	–50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	–4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	–8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	100	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	20	
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



# **SN74AHC08** **QUADRUPLE 2-INPUT POSITIVE-AND GATE**

SCLS236 – OCTOBER 1995

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
		4.5 V			0.36		0.44	
I <sub>I</sub>	A or B inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		± 0.1		± 1	µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		2		20	µA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10	10	pF

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	6.2	8.8		1	10.5	ns
t <sub>PHL</sub>				6.2	8.8		1	10.5	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	8.7	12.3		1	14	ns
t <sub>PHL</sub>				8.7	12.3		1	14	

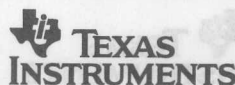
**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	4.3	5.9		1	7	ns
t <sub>PHL</sub>				4.3	5.9		1	7	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	5.8	7.9		1	9	ns
t <sub>PHL</sub>				5.8	7.9		1	9	

**noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 4)**

PARAMETER		MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>			0.8	V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>			-0.8	V
V <sub>IH(D)</sub>	High-level dynamic input voltage	3.5			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.



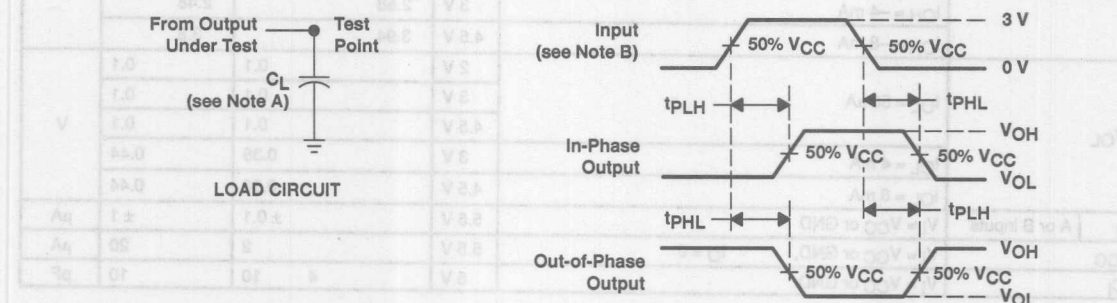
# SN74AHC08 QUADRUPLE 2-INPUT POSITIVE-AND GATE

SCLS236 – OCTOBER 1995

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	18	pF

## PARAMETER MEASUREMENT INFORMATION



## VOLTAGE WAVEFORMS DELAY TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CAPACITANCE	MIN	TYP	MAX	UNIT
$t_{PLH}$	A to B	Y	$C_L = 15\text{ pF}$	4.2	5.0	7.0	ns
$t_{PHL}$	A to B	Y	$C_L = 15\text{ pF}$	4.2	5.0	7.0	ns
$t_{PLH}$	A to B	Y	$C_L = 50\text{ pF}$	6.0	7.0	9.0	ns
$t_{PHL}$	A to B	Y	$C_L = 50\text{ pF}$	6.0	7.0	9.0	ns

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OH}$ High-level output voltage	3.5			V
$V_{OL}$ Low-level output voltage			0.5	V
$V_{IH}$ High-level input voltage			3.5	V
$V_{IL}$ Low-level input voltage			0.5	V

NOTE 4: Characteristics are determined during product characterization and measured by design for surface-mount packages only.



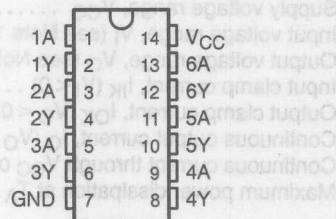
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# SN74AHC14 HEX SCHMITT-TRIGGER INVERTER

SCLS238A – OCTOBER 1995 – REVISED JANUARY 1996

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

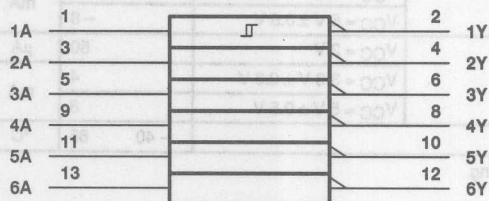
The SN74AHC14 contains six independent inverters. The device performs the Boolean function  $Y = \bar{A}$ . Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive- ( $V_{T+}$ ) and negative-going ( $V_{T-}$ ) signals.

The SN74AHC14 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each gate)

INPUT A	OUTPUT Y
H	L
L	H

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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# SN74AHC14

## HEX SCHMITT-TRIGGER INVERTER

SCLS238A – OCTOBER 1995 – REVISED JANUARY 1996

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V		–50
		$V_{CC} = 3.3$ V ± 0.3 V		–4
		$V_{CC} = 5$ V ± 0.5 V		–8
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V		50
		$V_{CC} = 3.3$ V ± 0.3 V		4
		$V_{CC} = 5$ V ± 0.5 V		8
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

# SN74AHC14 HEX SCHMITT-TRIGGER INVERTER

SCLS238A – OCTOBER 1995 – REVISED JANUARY 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>T+</sub> Positive-going input threshold voltage		3 V			2.2		2.2	V
		4.5 V			3.15		3.15	
		5.5 V			3.85		3.85	
V <sub>T-</sub> Negative-going input threshold voltage		3 V	0.9			0.9		V
		4.5 V	1.35			1.35		
		5.5 V	1.65			1.65		
$\Delta V_T$ Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )		3 V	0.3		1.2	0.3	1.2	V
		4.5 V	0.4		1.4	0.4	1.4	
		5.5 V	0.5		1.6	0.5	1.6	
V <sub>OH</sub>	I <sub>OH</sub> = -50 $\mu$ A	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 $\mu$ A	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			$\pm 0.1$		$\pm 1$	$\mu$ A
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20	$\mu$ A
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF		8.3	12.8	1	15	ns
t <sub>PHL</sub>					8.3	12.8	1	15	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF		10.8	16.3	1	18.5	ns
t <sub>PHL</sub>					10.8	16.3	1	18.5	

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V  $\pm$  0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF		5.5	8.6	1	10	ns
t <sub>PHL</sub>					5.5	8.6	1	10	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF		7	10.6	1	12	ns
t <sub>PHL</sub>					7	10.6	1	12	



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# SN74AHC14

## HEX SCHMITT-TRIGGER INVERTER

SCLS238A – OCTOBER 1995 – REVISED JANUARY 1996

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $t_r = t_f = 3\text{ ns}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

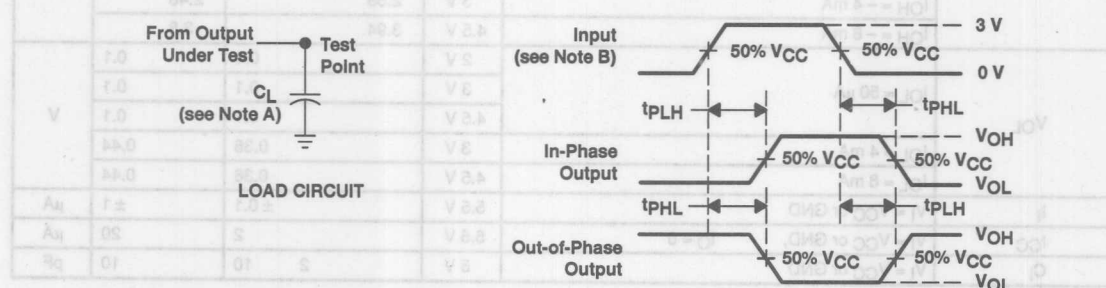
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.4		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	9	pF

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

UNIT	MIN	TYP	MAX	PARAMETER
ns	10	8.5	10	$t_{PLH}$
ns	10	8.5	10	$t_{PHL}$
ns	10	8.5	10	$t_{PLH}$
ns	10	8.5	10	$t_{PHL}$

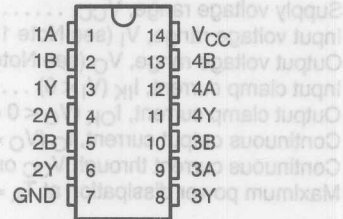


# SN74AHC32 QUADRUPE 2-INPUT POSITIVE-OR GATE

SCLS247 – OCTOBER 1995

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

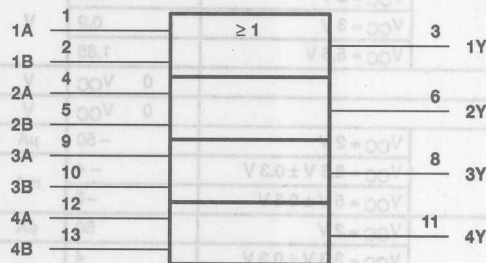
The SN74AHC32 is a quadruple 2-input positive-OR gate. The device performs the Boolean functions  $Y = \overline{A} \cdot \overline{B}$  or  $Y = A + B$  in positive logic.

The SN74AHC32 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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# SN74AHC32

## QUADRUPLE 2-INPUT POSITIVE-OR GATE

SCLS247 – OCTOBER 1995

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 3$ V	2.1	
		$V_{CC} = 5.5$ V	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 3$ V	0.9	
		$V_{CC} = 5.5$ V	1.65	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	–50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	–4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	–8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	100	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	20	
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

# SN74AHC32

## QUADRUPL 2-INPUT POSITIVE-OR GATE

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = – 50 µA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = – 4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = – 8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
I <sub>I</sub>	A or B inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		± 0.1		± 1	µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		2		20	µA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10		pF

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF		5.5	7.9	1	9.5	ns
t <sub>PHL</sub>					5.5	7.9	1	9.5	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF		8	11.4	1	13	ns
t <sub>PHL</sub>					8	11.4	1	13	

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF		3.8	5.5	1	6.5	ns
t <sub>PHL</sub>					3.8	5.5	1	6.5	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF		5.3	7.5	1	8.5	ns
t <sub>PHL</sub>					5.3	7.5	1	8.5	

noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.3	0.8	V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		–0.3	–0.8	V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>		4.7		V
V <sub>IH(D)</sub>	High-level dynamic input voltage	3.5			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

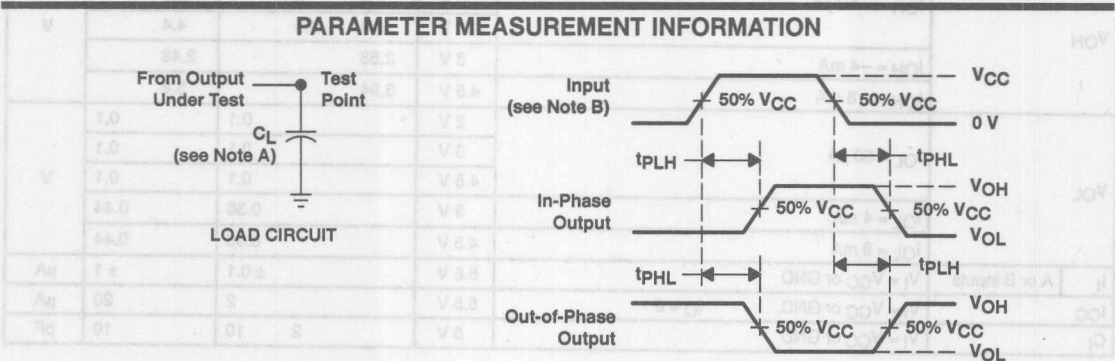


SN74AHC32  
QUADRUPLE 2-INPUT POSITIVE-OR GATE

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operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	14	pF



**VOLTAGE WAVEFORMS  
DELAY TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$	
				MIN	TYP MAX
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$	2.8	2.8 3.8
$t_{PHL}$	A or B	Y	$C_L = 50\text{ pF}$	2.8	2.8 3.8

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OH}$	Quiet output, minimum dynamic $V_{OH}$	2.8			V
$V_{OL}$	Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{IH}$	High-level dynamic input voltage			1.5	V
$V_{IL}$	Low-level dynamic input voltage			0.8	V

NOTE: Characteristics are determined during product characterization and are not guaranteed by design for surface-mount packages only.





# SN74AHC74

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

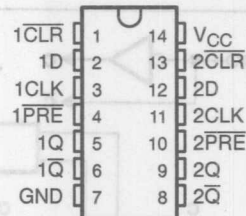
### description

The SN74AHC74 is a dual positive-edge-triggered D-type flip-flop.

A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) inputs sets or resets the outputs regardless of the levels of the other inputs. When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the D input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN74AHC74 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

D, DB, N, OR PW PACKAGE  
(TOP VIEW)

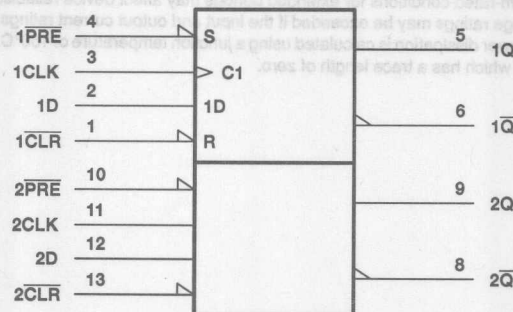


FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\overline{Q}_0$

<sup>†</sup> This configuration is nonstable; that is, it does not persist when  $\overline{PRE}$  or  $\overline{CLR}$  returns to its inactive (high) level.

### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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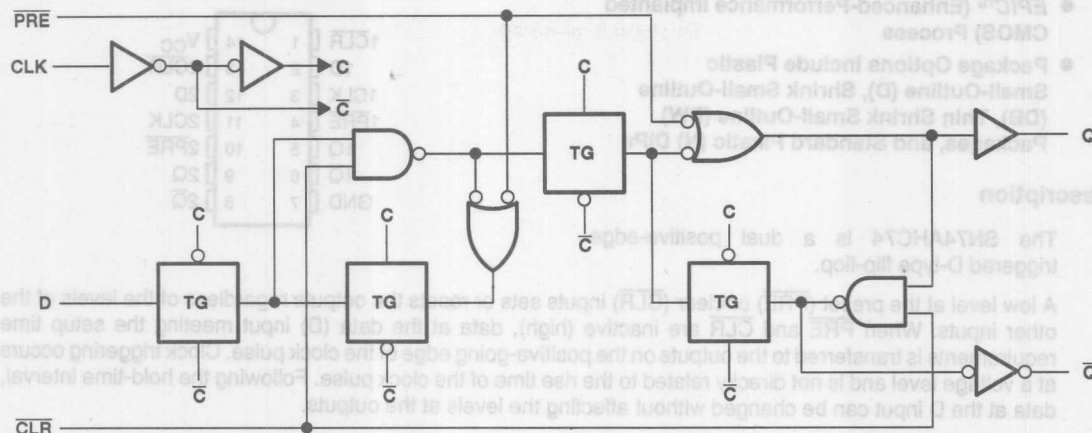
PRODUCT PREVIEW

# SN74AHC74

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCLS255 – DECEMBER 1995

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW

TEXAS  
INSTRUMENTS

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# SN74AHC74

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		V
		$V_{CC} = 3\text{ V}$	2.1		
		$V_{CC} = 5.5\text{ V}$	3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5	V
		$V_{CC} = 3\text{ V}$		0.9	
		$V_{CC} = 5.5\text{ V}$		1.65	
$V_I$	Input voltage		0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$		-50	$\mu\text{A}$
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		-4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		-8	
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$		50	$\mu\text{A}$
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		20	
$T_A$	Operating free-air temperature		-40	85	$^{\circ}\text{C}$

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^{\circ}\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50\text{ }\mu\text{A}$	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
$V_{OL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	$I_{OL} = 4\text{ mA}$	3 V			0.36		0.44	
		4.5 V			0.36		0.44	
$I_I$	Data inputs	$V_I = V_{CC}\text{ or GND}$	5.5 V		$\pm 0.1$		$\pm 1$	$\mu\text{A}$
	Control inputs				$\pm 0.1$		$\pm 1$	
$I_{CC}$	$V_I = V_{CC}\text{ or GND}, I_O = 0$	5.5 V			2		20	$\mu\text{A}$
$C_i$	$V_I = V_{CC}\text{ or GND}$	5 V		4	10		10	pF

PRODUCT PREVIEW



# SN74AHC74

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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timing requirements over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
$t_w$	Pulse duration	PRE or CLR low	6	7			ns
		CLK	6	7			
$t_{su}$	Setup time before CLK $\uparrow$	Data	6	7			ns
		PRE or CLR inactive	6	7			
$t_h$	Hold time, data after CLK $\uparrow$		0.5	0.5			ns
$t_{rem}$	Minimum removal time	PRE or CLR	5	5			ns

timing requirements over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
$t_w$	Pulse duration	PRE or CLR low	5	5			ns
		CLK	5	5			
$t_{su}$	Setup time before CLK $\uparrow$	Data	5	5			ns
		PRE or CLR inactive	5	5			
$t_h$	Hold time, data after CLK $\uparrow$		0.5	0.5			ns
$t_{rem}$	Minimum removal time	PRE or CLR	3	3			ns

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT			
				MIN	TYP	MAX						
f <sub>max</sub>	PRE or CLR	Q or Q̄	C <sub>L</sub> = 15 pF	80	125		70		MHz			
f <sub>max</sub>			C <sub>L</sub> = 50 pF	50	75		45					
t <sub>PLH</sub>			CLK	Q or Q̄	C <sub>L</sub> = 15 pF		7.6	12.3	1	14.5	ns	
t <sub>PHL</sub>							7.6	12.3	1	14.5		
t <sub>PLH</sub>	PRE or CLR	Q or Q̄				C <sub>L</sub> = 50 pF		6.7	11.9	1	14	ns
t <sub>PHL</sub>								6.7	11.9	1	14	
t <sub>PLH</sub>			CLK	Q or Q̄	C <sub>L</sub> = 50 pF			10.1	15.8	1	18	ns
t <sub>PHL</sub>								10.1	15.8	1	18	
t <sub>PLH</sub>	CLK	Q or Q̄				C <sub>L</sub> = 50 pF		9.2	15.4	1	17.5	ns
t <sub>PHL</sub>								9.2	15.4	1	17.5	

PRODUCT PREVIEW



# SN74AHC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCLS255 – DECEMBER 1995

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TA = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
fmax			CL = 15 pF	130	170		110		MHz
fmax			CL = 50 pF	90	115		75		
tPLH	PRE or CLR	Q or Q̄	CL = 15 pF	4.8	7.7		1	9	ns
tPHL				4.8	7.7		1	9	
tPLH	CLK	Q or Q̄		4.6	7.3		1	8.5	ns
tPHL				4.6	7.3		1	8.5	
tPLH	PRE or CLR	Q or Q̄	CL = 50 pF	6.3	9.7		1	11	ns
tPHL				6.3	9.7		1	11	
tPLH	CLK	Q or Q		6.1	9.3		1	10.5	ns
tPHL				6.1	9.3		1	10.5	

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$	$f = 1\text{ MHz}$		25		pF

PRODUCT PREVIEW

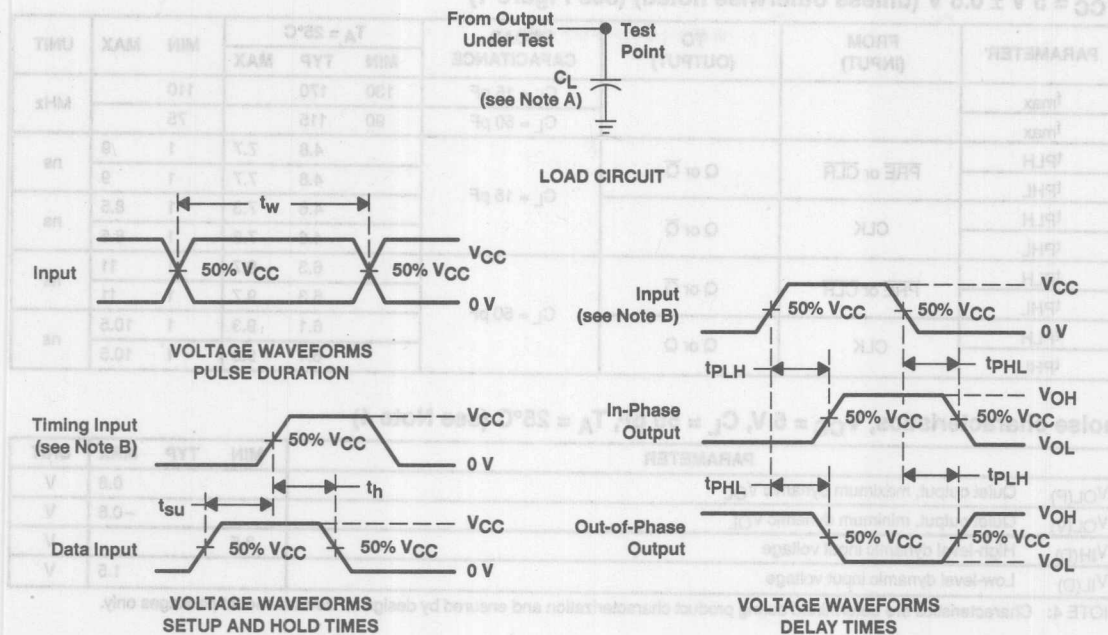




# **SN74AHC74** **DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP** **WITH CLEAR AND PRESET**

SCLS255 – DECEMBER 1995

## **PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PRODUCT PREVIEW



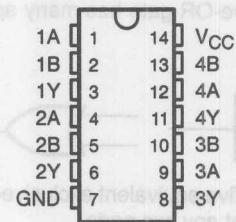
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# SN74AHC86 QUADRUPL 2-INPUT EXCLUSIVE-OR GATE

SCLS249 – OCTOBER 1995

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

The SN74AHC86 is a quadruple 2-input exclusive-OR gate. The device performs the Boolean functions  $Y = A \oplus B$  or  $Y = \bar{A}B + A\bar{B}$  in positive logic.

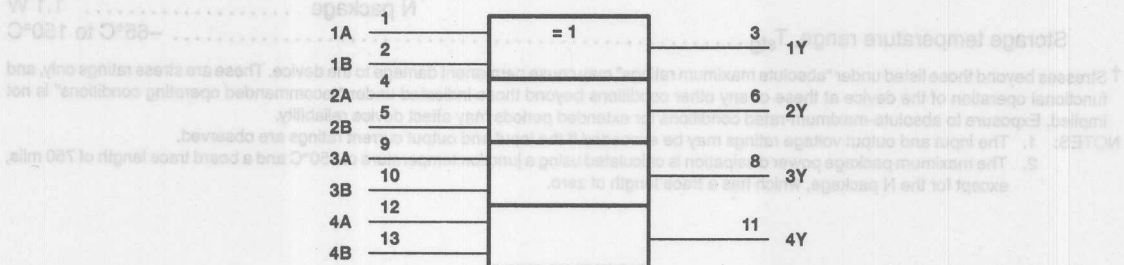
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The SN74AHC86 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
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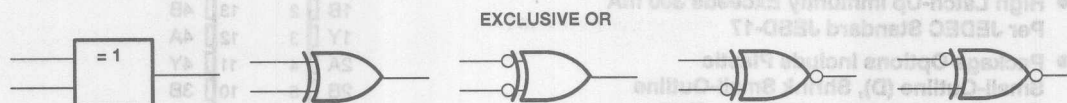
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# SN74AHC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCLS249 - OCTOBER 1995

## exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an SN74AHC86 gate in positive logic; negation may be shown at any two ports.

### LOGIC-IDENTITY ELEMENT



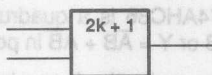
The output is active (low) if all inputs stand at the same logic level (i.e.,  $A = B$ ).

### EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

### ODD-PARITY ELEMENT



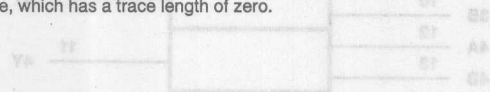
The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	.....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	.....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	.....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	.....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	.....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	.....	$\pm 50$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):		
	D package	1.25 W
	DB or PW package	0.5 W
	N package	1.1 W
Storage temperature range, $T_{stg}$	.....	$-65^\circ\text{C}$ to $150^\circ\text{C}$

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils, except for the N package, which has a trace length of zero.



**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN74AHC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCLS249 – OCTOBER 1995

## recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		V
		$V_{CC} = 3\text{ V}$	2.1		
		$V_{CC} = 5.5\text{ V}$	3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5	V
		$V_{CC} = 3\text{ V}$		0.9	
		$V_{CC} = 5.5\text{ V}$		1.65	
$V_I$	Input voltage		0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$		-50	$\mu\text{A}$
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		-4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		-8	
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$		50	$\mu\text{A}$
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		20	
$T_A$	Operating free-air temperature		-40	85	$^{\circ}\text{C}$

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$V_{CC}$	$T_A = 25^{\circ}\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$V_{OH}$		$I_{OH} = -50\text{ }\mu\text{A}$	2 V	1.9	2		1.9		V
			3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		
			4.5 V	3.94			3.8		
$V_{OL}$		$I_{OL} = 50\text{ }\mu\text{A}$	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		$I_{OL} = 4\text{ mA}$	3 V			0.36		0.44	
			4.5 V			0.36		0.44	
$I_I$	A or B inputs	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$	$\mu\text{A}$
$I_{CC}$		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	$\mu\text{A}$
$C_i$		$V_I = V_{CC}$ or GND	5 V		4	10		10	pF



# SN74AHC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$	7	11		1	13	ns
$t_{PHL}$				7	11		1	13	
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$	9.5	14.5		1	16.5	ns
$t_{PHL}$				9.5	14.5		1	16.5	

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$	4.8	6.8		1	8	ns
$t_{PHL}$				4.8	6.8		1	8	
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$	6.3	8.8		1	10	ns
$t_{PHL}$				6.3	8.8		1	10	

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.3	-0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

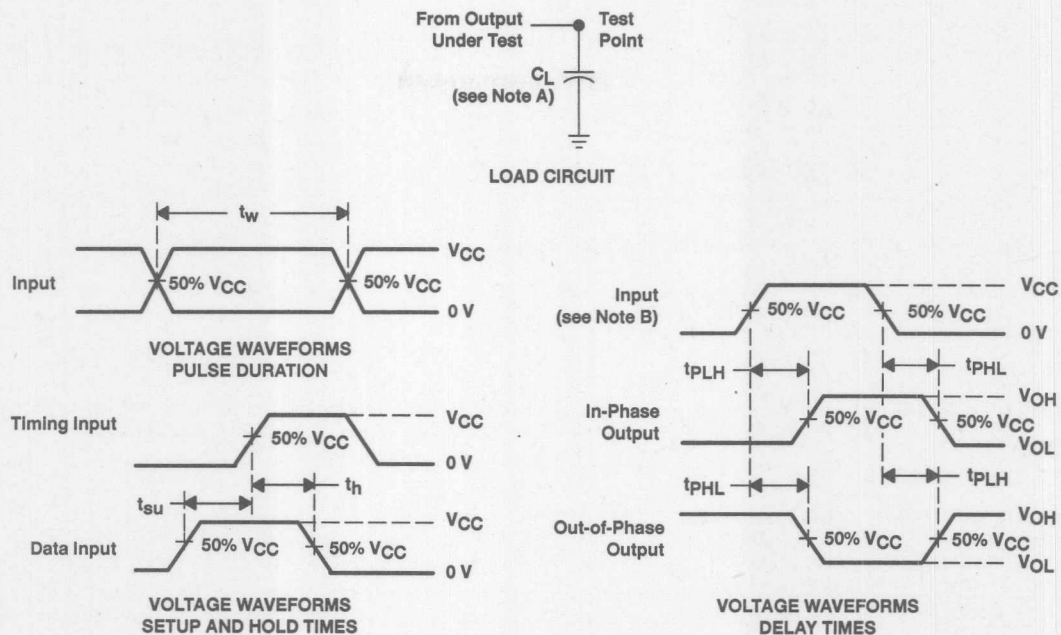
PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	18	pF

V	1.0	1.0	V <sub>OL</sub>	Am 6 = 10 <sup>1</sup>	
	1.0	1.0	V <sub>OL</sub>	Am 10 = 10 <sup>1</sup>	
	1.0	1.0	V <sub>OL</sub>	Am 1 = 10 <sup>1</sup>	
	1.0	1.0	V <sub>OL</sub>	Am 2 = 10 <sup>1</sup>	
	1.0	1.0	V <sub>OL</sub>	Am 3 = 10 <sup>1</sup>	
Am	1.0	1.0	V <sub>OL</sub>	Am 4 = 10 <sup>1</sup>	
Am	1.0	1.0	V <sub>OL</sub>	Am 5 = 10 <sup>1</sup>	
Am	1.0	1.0	V <sub>OL</sub>	Am 6 = 10 <sup>1</sup>	
Am	1.0	1.0	V <sub>OL</sub>	Am 7 = 10 <sup>1</sup>	
Am	1.0	1.0	V <sub>OL</sub>	Am 8 = 10 <sup>1</sup>	





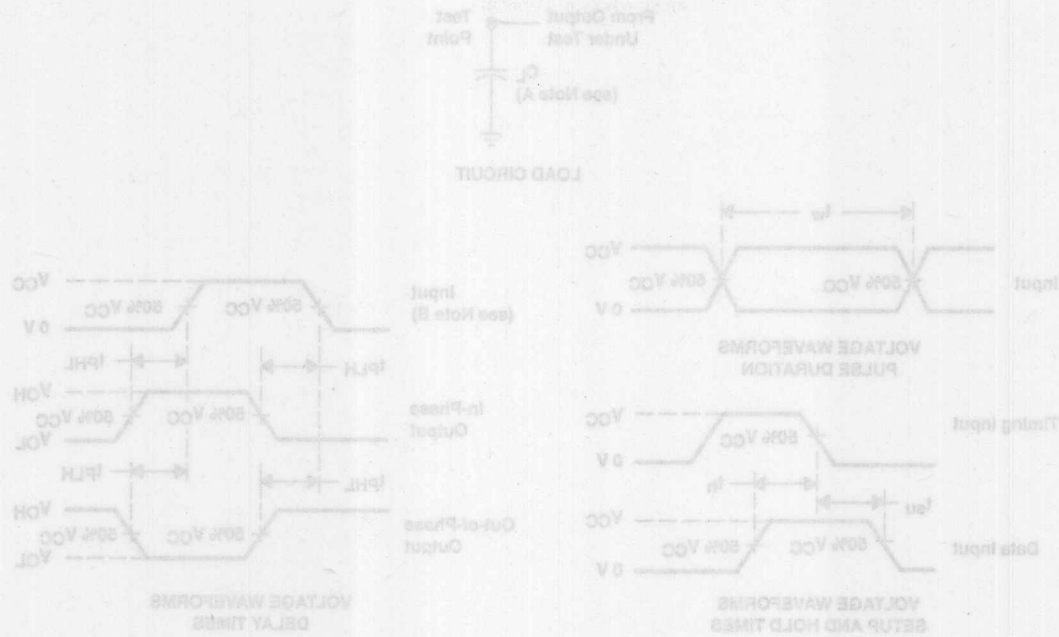
PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_0 = 50 \Omega$ ,  $V = 3$  V,  $t_r = 3$  ns.  
C. The outputs are measured one at a time with one input transition per measurement.

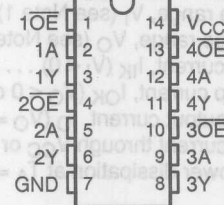
Figure 1. Load Circuit and Voltage Waveforms

# SN74AHC125 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCLS256 - DECEMBER 1995

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

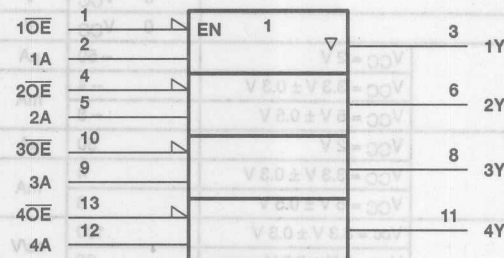
The SN74AHC125 quadruple bus buffer gate features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high. When  $\overline{OE}$  is low, the respective gate passes the data from the A input to its Y output.

The SN74AHC125 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each buffer)

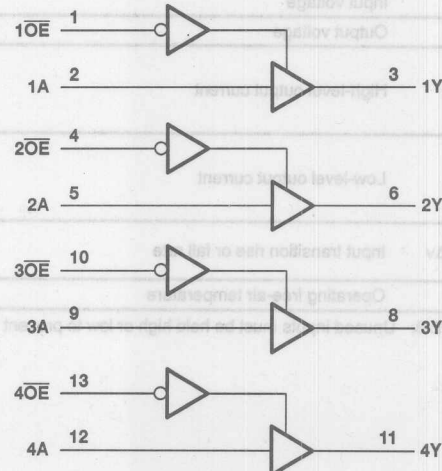
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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# **SN74AHC125** **QUADRUPLE BUS BUFFER GATE** **WITH 3-STATE OUTPUTS**

SCLS256 – DECEMBER 1995

## **absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W

Storage temperature range,  $T_{stg}$  ..... –65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## **recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 3$ V	2.1	
		$V_{CC} = 5.5$ V	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 3$ V	0.9	
		$V_{CC} = 5.5$ V	1.65	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	–50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	–4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	–8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	100	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	20	
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW



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**SN74AHC125**  
**QUADRUPLE BUS BUFFER GATE**  
**WITH 3-STATE OUTPUTS**  
SCLS256 – DECEMBER 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V			0.1	0.1		V
		3 V			0.1	0.1		
		4.5 V			0.1	0.1		
	I <sub>OL</sub> = 4 mA	3 V			0.36	0.44		
	I <sub>OL</sub> = 8 mA	4.5 V			0.36	0.44		
I <sub>I</sub>	A or $\overline{OE}$ inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		± 0.1	± 1		µA
I <sub>OZ</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		± 0.25	± 2.5		µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		2	20		µA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	4	10	10		pF

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF						ns
t <sub>PHL</sub>									
t <sub>PZH</sub>	OE	Y							ns
t <sub>PZL</sub>									
t <sub>PHZ</sub>	OE	Y							ns
t <sub>PLZ</sub>									
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF						ns
t <sub>PHL</sub>									
t <sub>PZH</sub>	OE	Y							ns
t <sub>PZL</sub>									
t <sub>PHZ</sub>	OE	Y							ns
t <sub>PLZ</sub>									

PRODUCT PREVIEW





SN74AHC125  
QUADRUPLE BUS BUFFER GATE  
WITH 3-STATE OUTPUTS

SCLS256 – DECEMBER 1995

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
				MIN	TYP	MAX				
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF						ns	
t <sub>PHL</sub>										
t <sub>PZH</sub>	OE	Y							ns	
t <sub>PZL</sub>										
t <sub>PHZ</sub>	OE	Y	C <sub>L</sub> = 50 pF						ns	
t <sub>PLZ</sub>										
t <sub>PLH</sub>	A	Y							ns	
t <sub>PHL</sub>										
t <sub>PZH</sub>	OE	Y							ns	
t <sub>PZL</sub>										
t <sub>PHZ</sub>	OE	Y							ns	
t <sub>PLZ</sub>										

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	$3.3\text{ V} \pm 0.3\text{ V}$			1.5		1.5	ns
			$5\text{ V} \pm 0.5\text{ V}$			1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

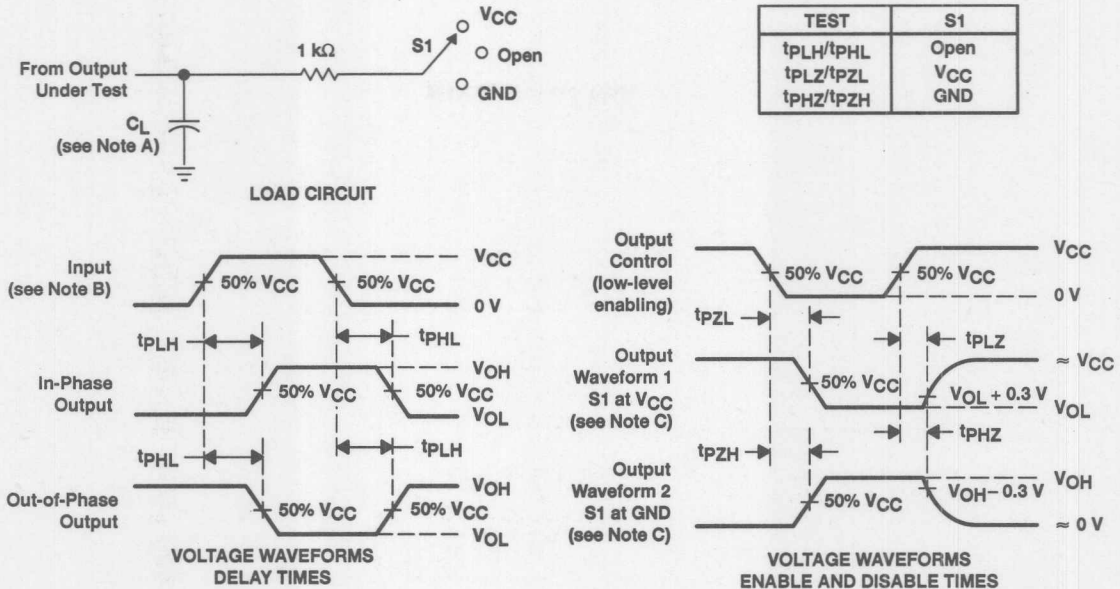
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ ,	$f = 1\text{ MHz}$				pF

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# PARAMETER MEASUREMENT INFORMATION



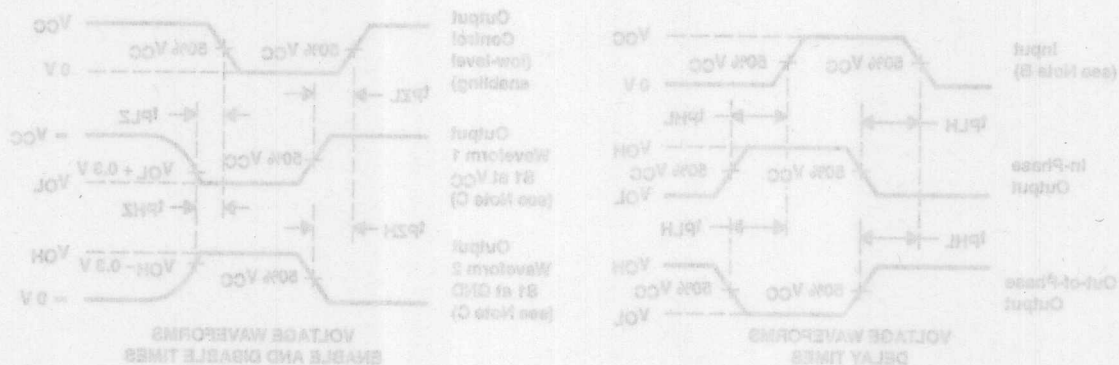
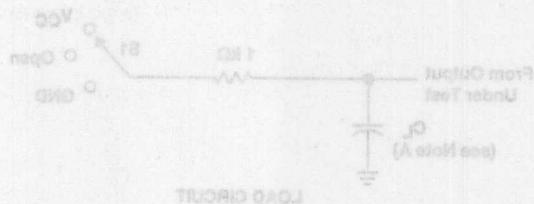
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

TEST	SI
Input High	Open
Input Low	VCC
Output High	GND



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_0 = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
D. The outputs are measured one at a time with one input transition per measurement.

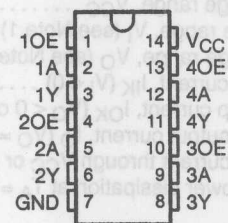
Figure 1. Load Circuit and Voltage Waveforms

WAVEFORM PREVIEW

**SN74AHC126**  
**QUADRUPLE BUS BUFFER GATE**  
**WITH 3-STATE OUTPUTS**  
SCLS257 – DECEMBER 1995

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



### description

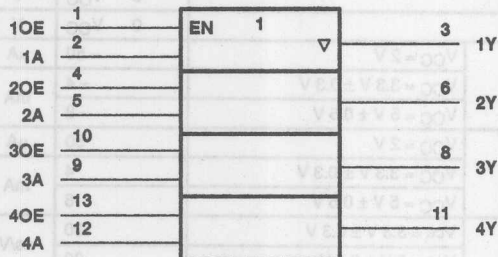
The SN74AHC126 quadruple bus buffer gate features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low. When OE is high, the respective gate passes the data from the A input to its Y output.

The SN74AHC126 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each buffer)

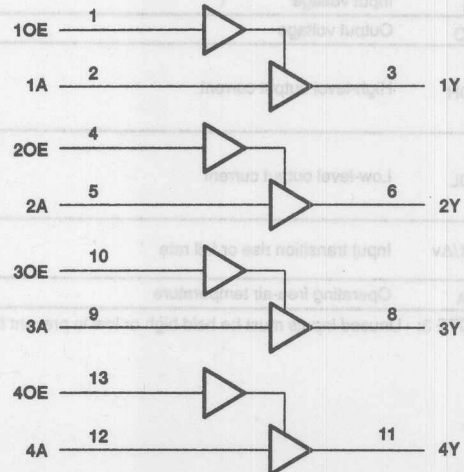
INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



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# SN74AHC126 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 3$ V	2.1	
		$V_{CC} = 5.5$ V	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 3$ V	0.9	
		$V_{CC} = 5.5$ V	1.65	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	–50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	–4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	–8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	100	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	20	
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW



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**SN74AHC126**  
**QUADRUPLE BUS BUFFER GATE**  
**WITH 3-STATE OUTPUTS**  
SCLS257 – DECEMBER 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = – 50 µA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = – 4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = – 8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V			0.1	0.1		V
		3 V			0.1	0.1		
		4.5 V			0.1	0.1		
	I <sub>OL</sub> = 4 mA	3 V			0.36	0.44		
	I <sub>OL</sub> = 8 mA	4.5 V			0.36	0.44		
I <sub>I</sub>	A or OE inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		± 0.1	± 1		µA
I <sub>OZ</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		± 0.25	± 2.5		µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			20		µA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	4	10		10	pF

switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF						ns
t <sub>PHL</sub>									
t <sub>PZH</sub>	OE	Y							ns
t <sub>PZL</sub>									
t <sub>PHZ</sub>	OE	Y							ns
t <sub>PLZ</sub>									
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF						ns
t <sub>PHL</sub>									
t <sub>PZH</sub>	OE	Y							ns
t <sub>PZL</sub>									
t <sub>PHZ</sub>	OE	Y							ns
t <sub>PLZ</sub>									

PRODUCT PREVIEW



# SN74AHC126 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCLS257 – DECEMBER 1995

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
				MIN	TYP	MAX				
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF						ns	
t <sub>PHL</sub>										
t <sub>PZH</sub>	OE	Y							ns	
t <sub>PZL</sub>										
t <sub>PHZ</sub>	OE	Y	C <sub>L</sub> = 50 pF						ns	
t <sub>PLZ</sub>										
t <sub>PLH</sub>	A	Y							ns	
t <sub>PHL</sub>										
t <sub>PZH</sub>	OE	Y							ns	
t <sub>PZL</sub>										
t <sub>PHZ</sub>	OE	Y							ns	
t <sub>PLZ</sub>										

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	$3.3\text{ V} \pm 0.3\text{ V}$			1.5		1.5	ns
			$5\text{ V} \pm 0.5\text{ V}$			1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

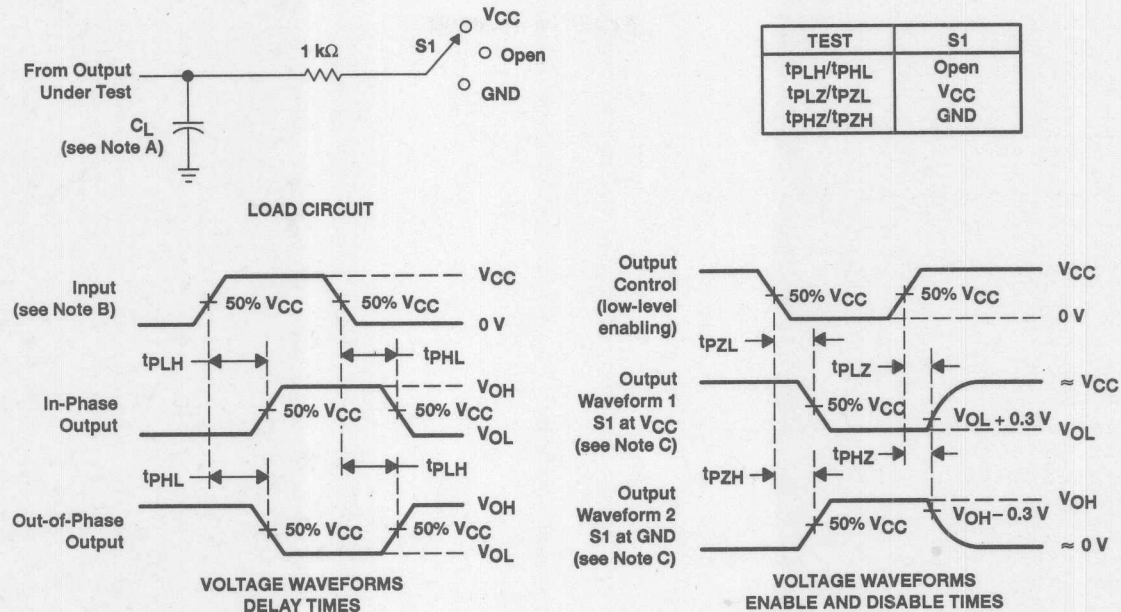
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ ,	$f = 1\text{ MHz}$				pF

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### PARAMETER MEASUREMENT INFORMATION



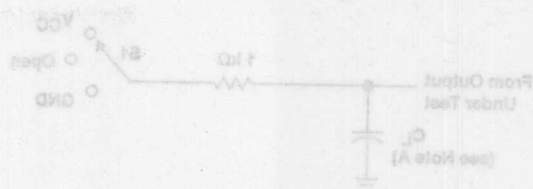
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

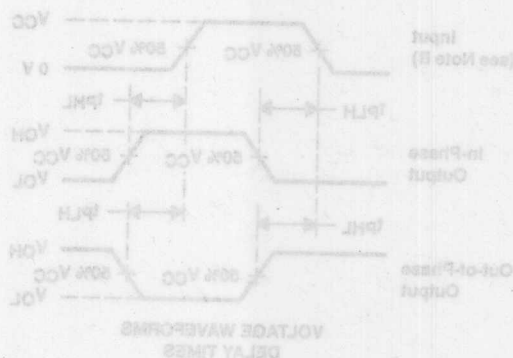
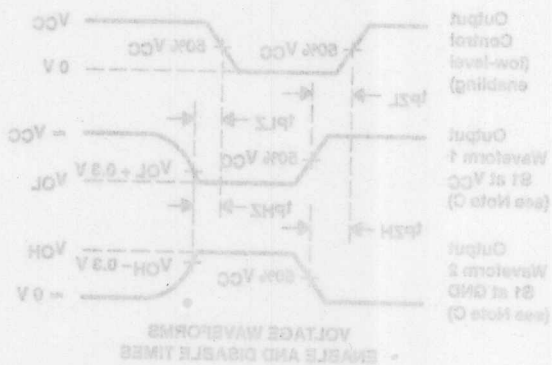
**PRODUCT PREVIEW**

# PARAMETER MEASUREMENT INFORMATION

TEST	SI
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZH}$	VCC
$t_{PHZ}/t_{PHZ}$	GND



LOAD CIRCUIT



NOTE: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
D. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
E. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

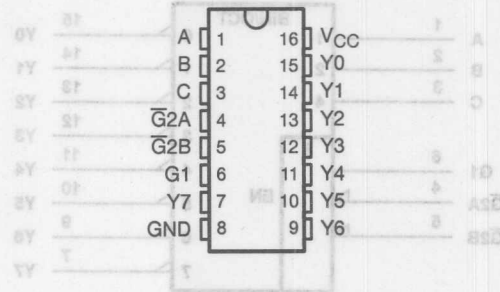
WAVEFORM REVIEW

# SN74AHC138 3-LINE TO 8-LINE DECODER/DEMULTIPLXER

SCLS258A – DECEMBER 1995 – REVISED JANUARY 1996

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporates Three Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

The SN74AHC138 decoder/demultiplexer is designed for high-performance memory-decoding or data-routing applications requiring very short propagation-delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN74AHC138 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

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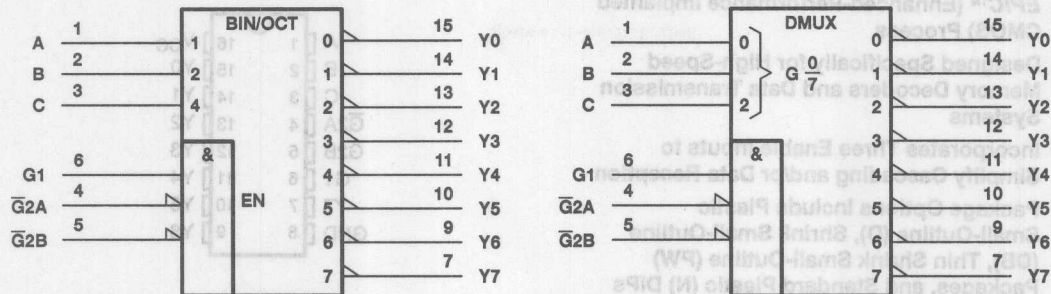
PRODUCT PREVIEW



# SN74AHC138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

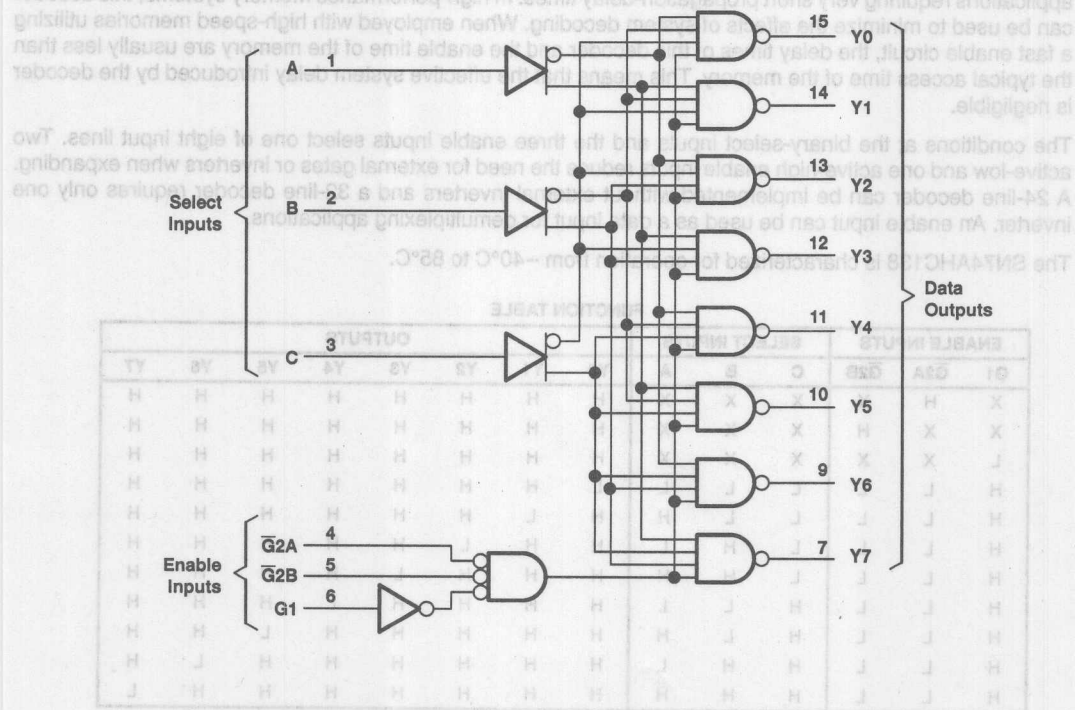
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## logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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SN74AHC138  
3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.3 W
DB package	0.55 W
N package	1.1 W
PW package	0.5 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 3$ V	2.1	
		$V_{CC} = 5.5$ V	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 3$ V	0.9	
		$V_{CC} = 5.5$ V	1.65	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	–50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	–4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	–8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	100	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	20	
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW



# SN74AHC138

## 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = – 50 µA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = – 4 mA	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
		4.5 V			0.36		0.44	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			± 0.1		± 1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10		10	pF

switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A, B, C	Any Y	C <sub>L</sub> = 15 pF	8.2	11.4	1	13	ns	
t <sub>PHL</sub>				8.2	11.4	1	13		
t <sub>PLH</sub>	G1	Any Y		8.1	12.8	1	15	ns	
t <sub>PHL</sub>				8.1	12.8	1	15		
t <sub>PLH</sub>	$\overline{G}2A, \overline{G}2B$	Any Y		8.2	11.4	1	13.5	ns	
t <sub>PHL</sub>				8.2	11.4	1	13.5		
t <sub>PLH</sub>	A, B, C	Any Y	C <sub>L</sub> = 50 pF	10	15.8	1	18	ns	
t <sub>PHL</sub>				10	15.8	1	18		
t <sub>PLH</sub>	G1	Any Y		10.6	16.3	1	18.5	ns	
t <sub>PHL</sub>				10.6	16.3	1	18.5		
t <sub>PLH</sub>	$\overline{G}2A, \overline{G}2B$	Any Y		10.7	14.9	1	17	ns	
t <sub>PHL</sub>				10.7	14.9	1	17		

V <sub>CC</sub>	5.0	V <sub>CC</sub> = 3.3 V ± 0.3 V	
V <sub>CC</sub>	0.5	V <sub>CC</sub> = 3.3 V ± 0.3 V	
T <sub>A</sub>	0	0	

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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# SN74AHC138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

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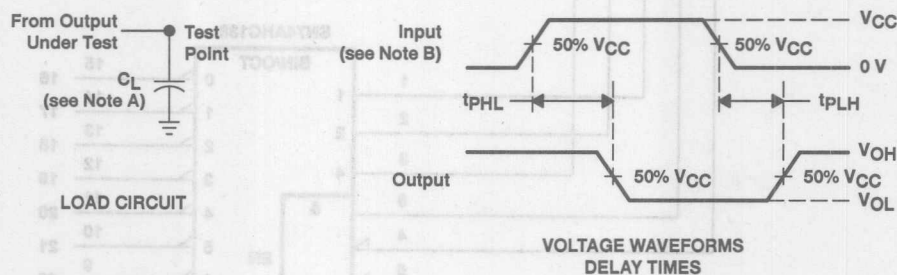
switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A, B, C	Any Y	C <sub>L</sub> = 15 pF	5.7	8.1	1	9.5	ns	
t <sub>PHL</sub>				5.7	8.1	1	9.5		
t <sub>PLH</sub>	G1	Any Y		5.6	8.1	1	9.5	ns	
t <sub>PHL</sub>				5.6	8.1	1	9.5		
t <sub>PLH</sub>	G̅2A, G̅2B	Any Y		5.8	8.1	1	9.5	ns	
t <sub>PHL</sub>				5.8	8.1	1	9.5		
t <sub>PLH</sub>	A, B, C	Any Y	C <sub>L</sub> = 50 pF	7.2	10.1	1	11.5	ns	
t <sub>PHL</sub>				7.2	10.1	1	11.5		
t <sub>PLH</sub>	G1	Any Y		7.1	10.1	1	11.5	ns	
t <sub>PHL</sub>				7.1	10.1	1	11.5		
t <sub>PLH</sub>	G̅2A, G̅2B	Any Y		7.3	10.1	1	11.5	ns	
t <sub>PHL</sub>				7.3	10.1	1	11.5		

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per gate	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	34	pF

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# SN74AHC138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

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## APPLICATION INFORMATION

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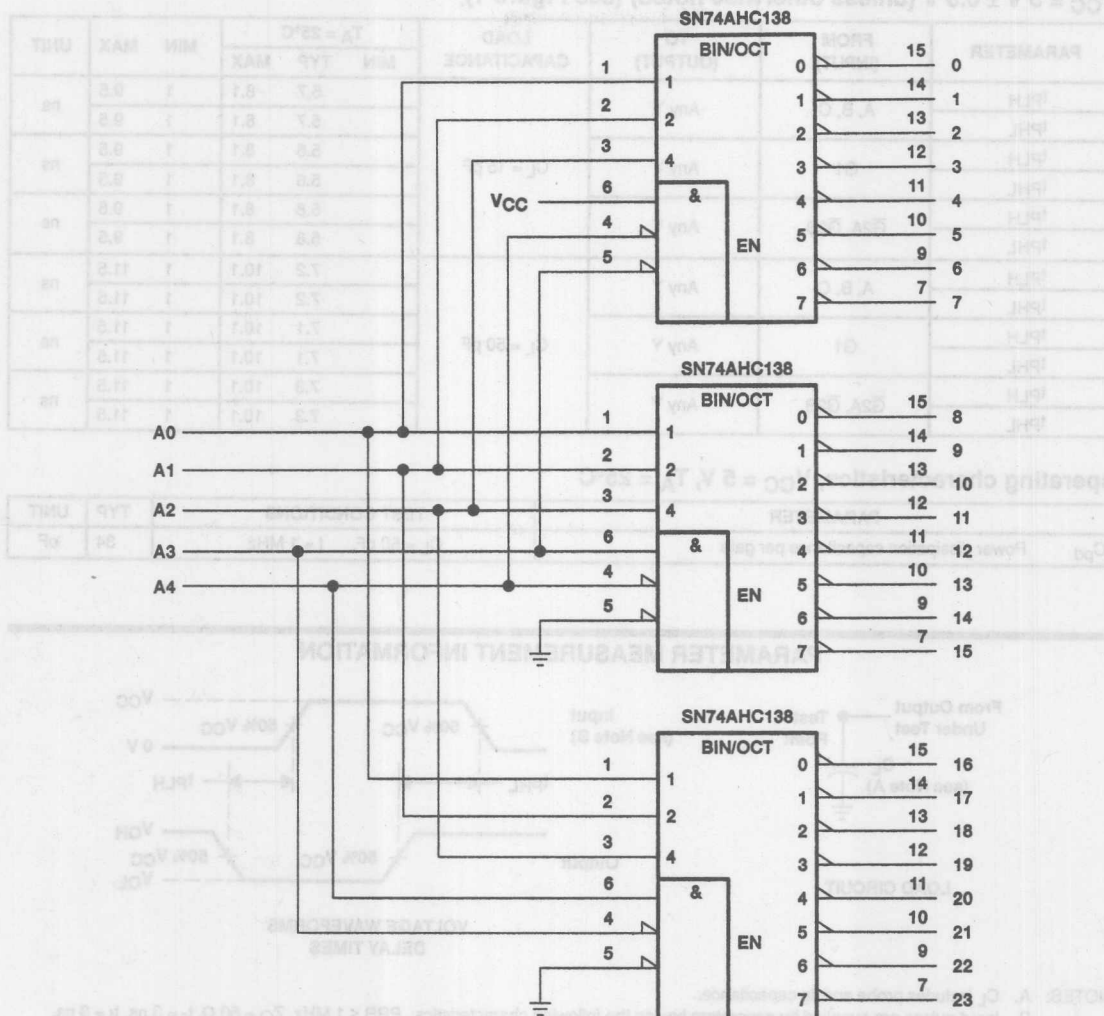


Figure 2. 24-Bit Decoding Scheme



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## APPLICATION INFORMATION

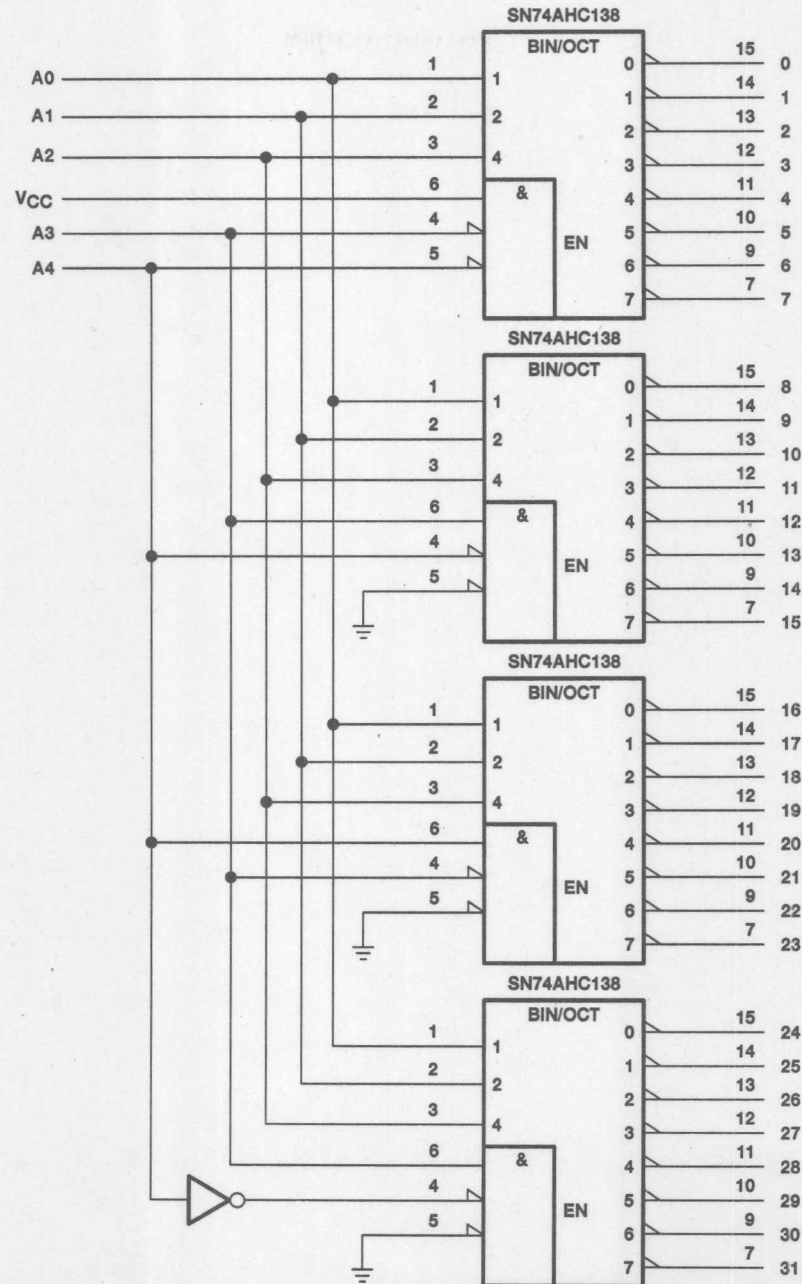


Figure 3. 32-Bit Decoding Scheme

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APPLICATION INFORMATION

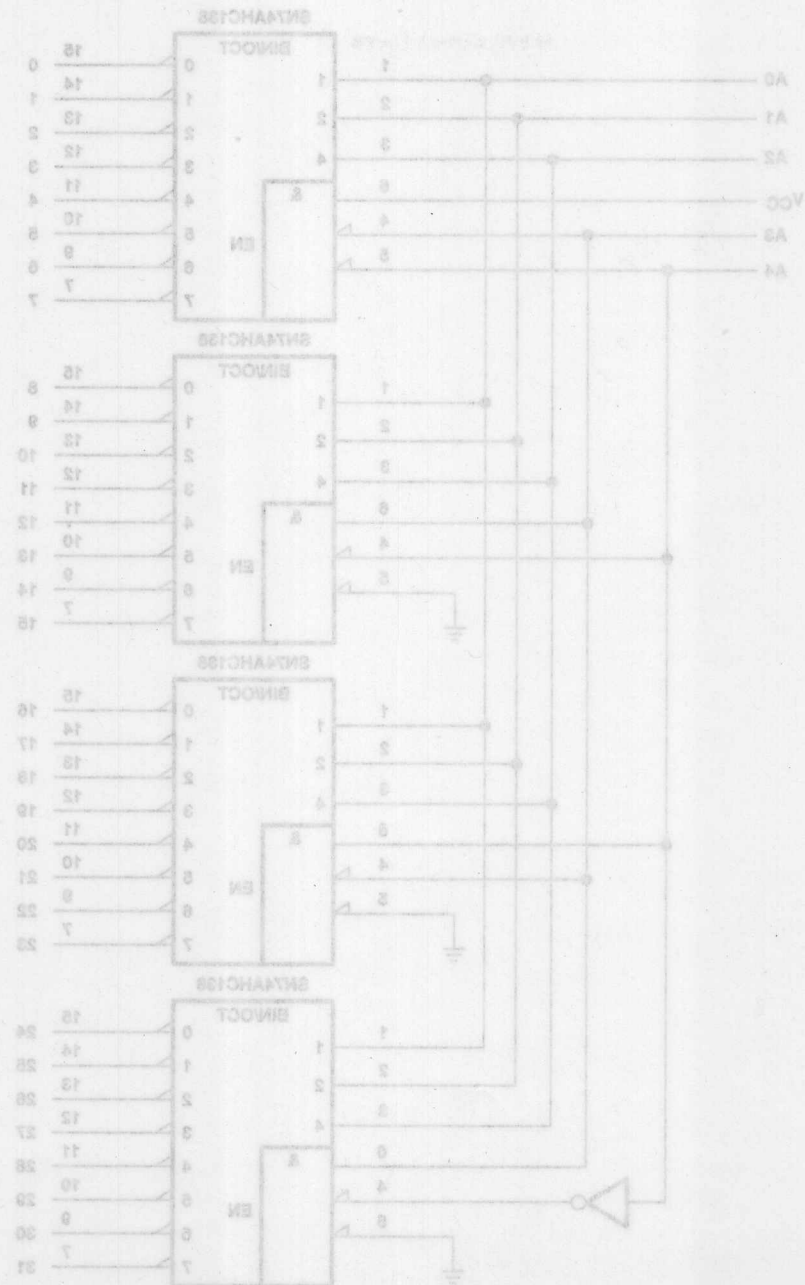


Figure 2. 32-Bit Decoding Scheme

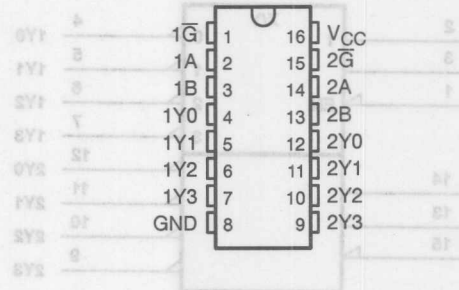
PRODUCT REVIEW

# SN74AHC139 DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCLS259B – DECEMBER 1995 – REVISED FEBRUARY 1996

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporates Two Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

The SN74AHC139 is a dual 2-line to 4-line decoder/demultiplexer designed for 2-V to 5.5-V  $V_{CC}$  operation. This device is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The active-low enable ( $\bar{G}$ ) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN74AHC139 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS			OUTPUTS			
$\bar{G}$	SELECT					
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

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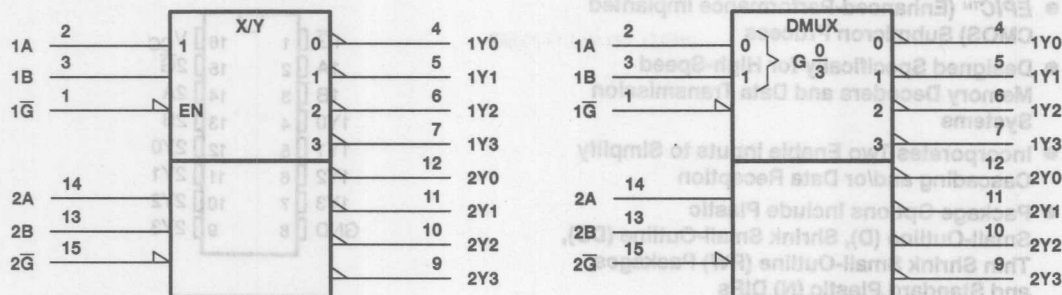
PRODUCT PREVIEW

# SN74AHC139

## DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

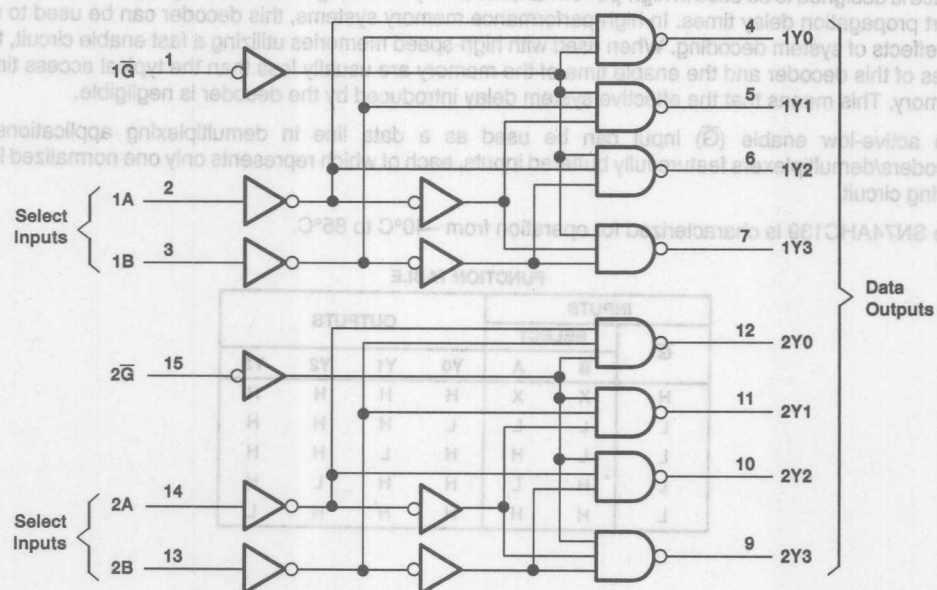
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### logic symbols (alternatives)<sup>†</sup>



<sup>†</sup> These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



PRODUCT PREVIEW

**TEXAS  
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# SN74AHC139

## DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.3 W
DB package	0.55 W
N package	1.1 W
PW package	0.5 W

Storage temperature range,  $T_{stg}$  –65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 3$ V	2.1	
		$V_{CC} = 5.5$ V	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 3$ V	0.9	
		$V_{CC} = 5.5$ V	1.65	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	–50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	–4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	–8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	100	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	20	
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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# SN74AHC139

## DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	4.5 V	3.94			3.8		V
		2 V			0.1		0.1	
		3 V			0.1		0.1	
	I <sub>OL</sub> = 4 mA	4.5 V			0.1		0.1	
	I <sub>OL</sub> = 8 mA	3 V			0.36		0.44	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	4.5 V			±0.1		±1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	µA
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10		10	pF

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF		7.2	11	1	13	ns
t <sub>PHL</sub>					7.2	11	1	13	
t <sub>PLH</sub>	$\bar{G}$	Y	C <sub>L</sub> = 15 pF		6.4	9.2	1	11	ns
t <sub>PHL</sub>					6.4	9.2	1	11	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF		9.7	14.5	1	16.5	ns
t <sub>PHL</sub>					9.7	14.5	1	16.5	
t <sub>PLH</sub>	$\bar{G}$	Y	C <sub>L</sub> = 50 pF		8.9	12.7	1	14.5	ns
t <sub>PHL</sub>					8.9	12.7	1	14.5	

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF		5	7.2	1	8.5	ns
t <sub>PHL</sub>					5	7.2	1	8.5	
t <sub>PLH</sub>	$\bar{G}$	Y	C <sub>L</sub> = 15 pF		4.4	6.3	1	7.5	ns
t <sub>PHL</sub>					4.4	6.3	1	7.5	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF		6.5	9.2	1	10.5	ns
t <sub>PHL</sub>					6.5	9.2	1	10.5	
t <sub>PLH</sub>	$\bar{G}$	Y	C <sub>L</sub> = 50 pF		5.9	8.3	1	9.5	ns
t <sub>PHL</sub>					5.9	8.3	1	9.5	



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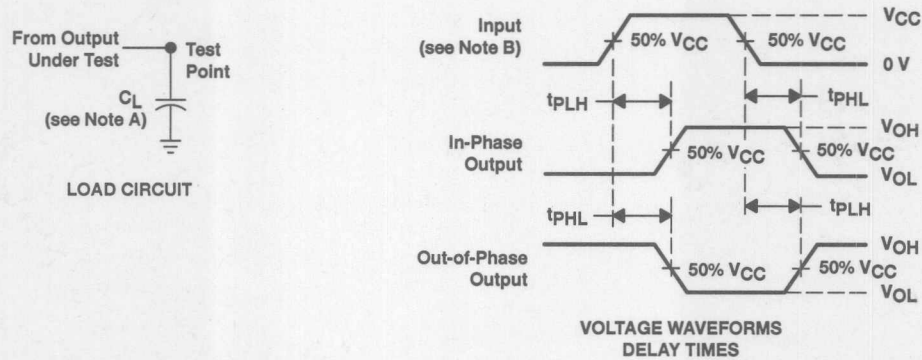
# SN74AHC139 DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCLS259B – DECEMBER 1995 – REVISED FEBRUARY 1996

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per gate	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	26	pF

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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Operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	UNIT
Power dissipation (maximum per gate)	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	W
$C_{PD}$		pF

PARAMETER MEASUREMENT INFORMATION

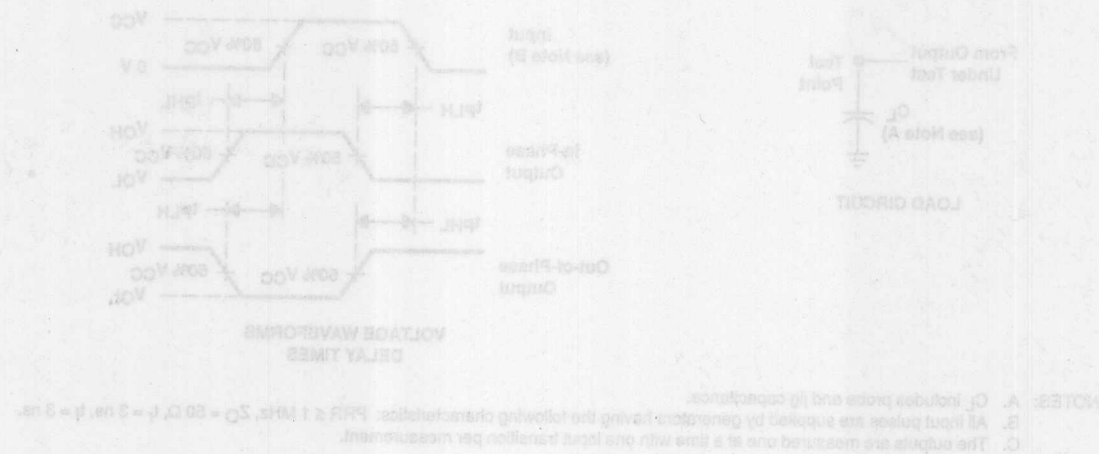


Figure 1. Load Circuit and Voltage Waveforms

# SN74AHC240

## OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Standard Plastic (N) DIPs

### description

This octal buffer/driver is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

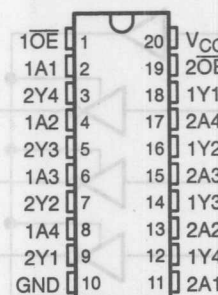
The SN74AHC240 is organized as two 4-bit buffers/line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The SN74AHC240 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

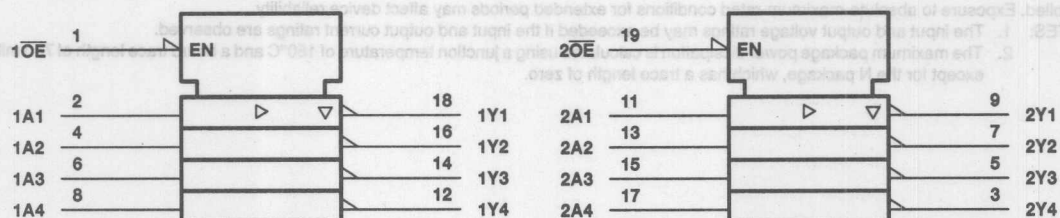
FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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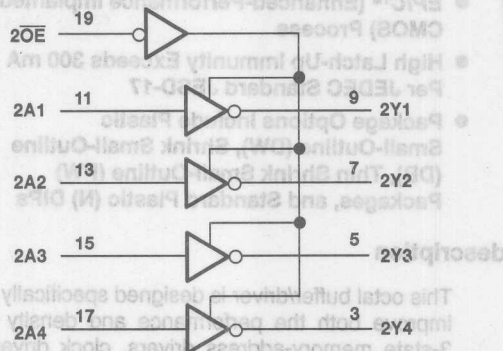
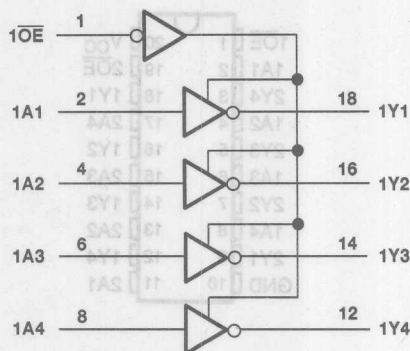
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# SN74AHC240 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



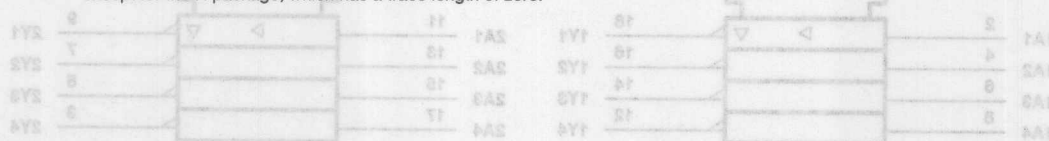
## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.





**SN74AHC240**  
**OCTAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**  
SCLS251 – OCTOBER 1995

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	V
		$V_{CC} = 3\text{ V}$	2.1	
		$V_{CC} = 5.5\text{ V}$	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	V
		$V_{CC} = 3\text{ V}$	0.9	
		$V_{CC} = 5.5\text{ V}$	1.65	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$	-50	$\mu\text{A}$
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	-4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	-8	
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$	50	$\mu\text{A}$
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	20	
$T_A$	Operating free-air temperature	-40	85	$^{\circ}\text{C}$

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V <sub>OH</sub>			2 V	1.9	2		1.9	V	
		I <sub>OH</sub> = -50 μA	3 V	2.9	3		2.9		
			4.5 V	4.4	4.5		4.4		
		I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
		I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>			2 V			0.1	0.1	V	
		I <sub>OL</sub> = 50 μA	3 V			0.1	0.1		
			4.5 V			0.1	0.1		
		I <sub>OL</sub> = 4 mA	3 V			0.36	0.44		
		I <sub>OL</sub> = 8 mA	4.5 V			0.36	0.44		
I <sub>I</sub>	Data inputs		5.5 V				±0.1	±1	μA
	Control inputs			V <sub>I</sub> = V <sub>CC</sub> or GND			±0.1	±1	
I <sub>OZ</sub> <sup>†</sup>		V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> (OE) = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V				±0.25	±2.5	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V				4	40	μA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	2.5 10				10	pF
C <sub>o</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	5 V	3.5					pF

$\dagger$  The parameter  $I_{OZ}$  includes the input leakage current.

# SN74AHC240

## OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A	Y	$C_L = 15 \text{ pF}$	5.3	7.5	1	9	ns	
$t_{PHL}$				5.3	7.5	1	9		
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 15 \text{ pF}$	6.6	10.6	1	12.5	ns	
$t_{PZL}$				6.6	10.6	1	12.5		
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 15 \text{ pF}$	7.8	11.5	1	12.5	ns	
$t_{PLZ}$				7.8	11.5	1	12.5		
$t_{PLH}$	A	Y	$C_L = 50 \text{ pF}$	7.8	11	1	12.5	ns	
$t_{PHL}$				7.8	11	1	12.5		
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50 \text{ pF}$	9.1	14.1	1	16	ns	
$t_{PZL}$				9.1	14.1	1	16		
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50 \text{ pF}$	10.3	14	1	16	ns	
$t_{PLZ}$				10.3	14	1	16		

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A	Y	$C_L = 15 \text{ pF}$	3.6	5.5	1	6.5	ns	
$t_{PHL}$				3.6	5.5	1	6.5		
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 15 \text{ pF}$	4.7	7.3	1	8.5	ns	
$t_{PZL}$				4.7	7.3	1	8.5		
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 15 \text{ pF}$	5.2	7.2	1	8.5	ns	
$t_{PLZ}$				5.2	7.2	1	8.5		
$t_{PLH}$	A	Y	$C_L = 50 \text{ pF}$	5.1	7.5	1	8.5	ns	
$t_{PHL}$				5.1	7.5	1	8.5		
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50 \text{ pF}$	6.2	9.3	1	10.5	ns	
$t_{PZL}$				6.2	9.3	1	10.5		
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50 \text{ pF}$	6.7	9.2	1	10.5	ns	
$t_{PLZ}$				6.7	9.2	1	10.5		

output-skew characteristics,  $C_L = 50 \text{ pF}$  (see Note 4)

PARAMETER	$V_{CC}$	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_{sk(o)}$ Output skew	$3.3 \text{ V} \pm 0.3 \text{ V}$	1.5	1.5	1	1	ns
	$5 \text{ V} \pm 0.5 \text{ V}$	1	1	1	1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.



noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

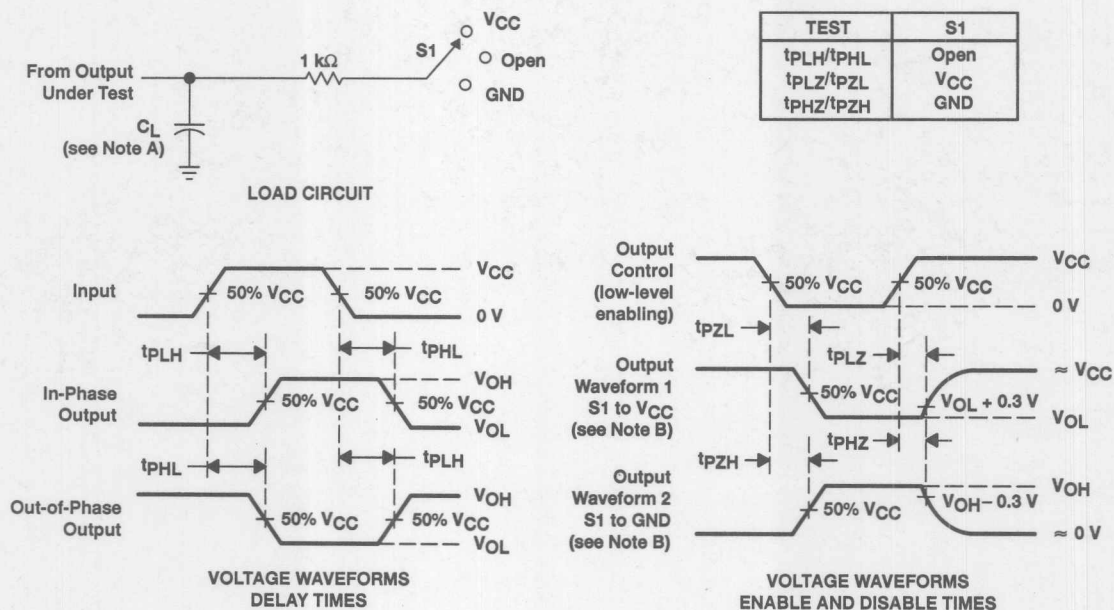
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	10	pF

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note B)

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OLP}$ Quiet output, maximum dynamic $V_{OL}$		0.5		V
$V_{OLN}$ Quiet output, minimum dynamic $V_{OL}$		-0.5		V
$V_{OHV}$ Quiet output, minimum dynamic $V_{OH}$		4.5		V
$V_{IHD}$ High-level dynamic input voltage	3.5			V
$V_{ILD}$ Low-level dynamic input voltage	1.5			V

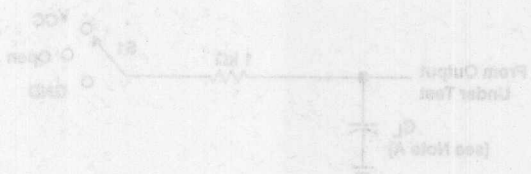
NOTE 8: Characteristics are determined during product characterization and stored by design for subsequent releases only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

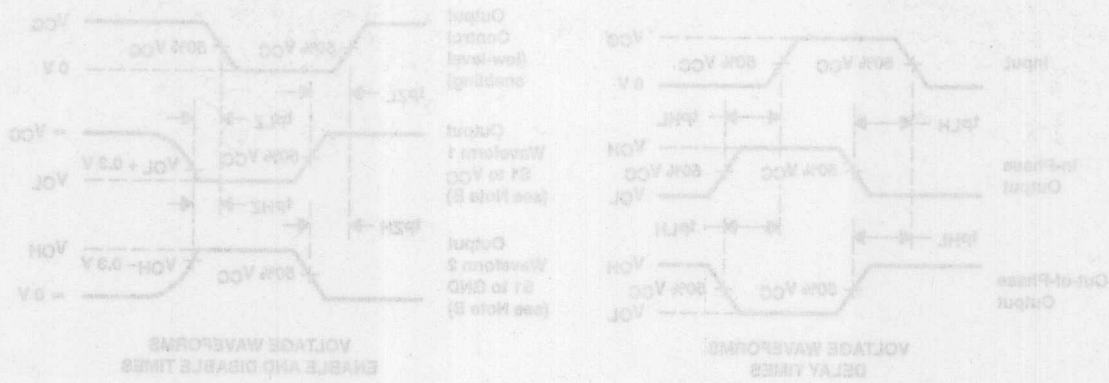
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{DD}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	10	pF

### PARAMETER MEASUREMENT INFORMATION

TEST	B1
Input High	Open
Input Low	$V_{CC}$
Input High	Open



LOAD CIRCUIT



NOTES:  
A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. All input signals are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $V_L = 0.5\text{ V}$ ,  $V_H = 4.5\text{ V}$ .  
E. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# SN74AHC244 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCLS226B – OCTOBER 1995 – REVISED FEBRUARY 1996

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

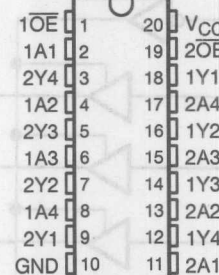
## description

This octal buffer/driver is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74AHC244 is organized as two 4-bit buffers/line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The SN74AHC244 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

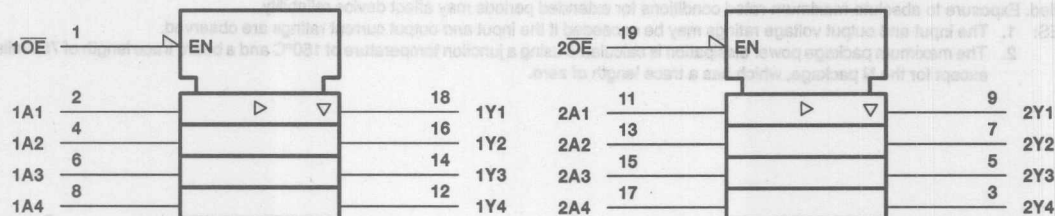
DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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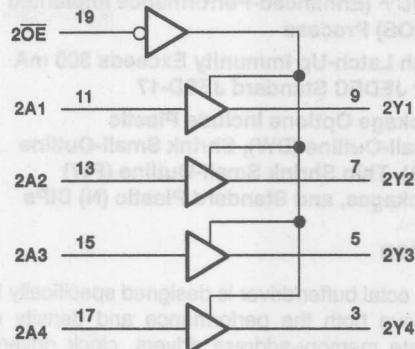
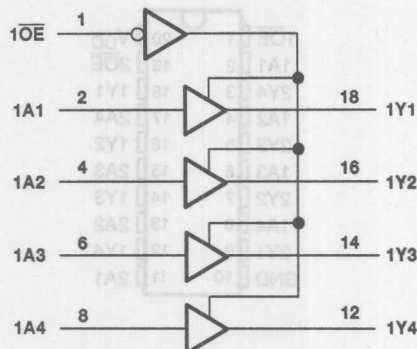
# SN74AHC244

## OCTAL BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

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#### logic diagram (positive logic)

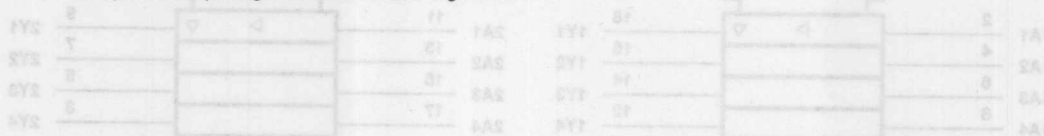


#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±25 mA
Continuous current through $V_{CC}$ or GND .....	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package .....	0.6 W
..... DW package .....	1.6 W
..... N package .....	1.3 W
..... PW package .....	0.7 W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.



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**SN74AHC244**  
**OCTAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

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**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	V
		$V_{CC} = 3\text{ V}$	2.1	
		$V_{CC} = 5.5\text{ V}$	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	V
		$V_{CC} = 3\text{ V}$	0.9	
		$V_{CC} = 5.5\text{ V}$	1.65	
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$	-50	$\mu\text{A}$
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	-4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	-8	
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$	50	$\mu\text{A}$
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	20	
$T_A$	Operating free-air temperature	-40	85	$^{\circ}\text{C}$

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^{\circ}\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50\text{ }\mu\text{A}$	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		
	$I_{OH} = -8\text{ mA}$	4.5 V	3.94			3.8		
$V_{OL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	$I_{OL} = 4\text{ mA}$	3 V			0.36		0.44	
	$I_{OL} = 8\text{ mA}$	4.5 V			0.36		0.44	
$I_I$	Data inputs	5.5 V	$V_I = V_{CC}$ or GND			$\pm 0.1$	$\pm 1$	$\mu\text{A}$
	Control inputs		$V_I = V_{CC}$ or GND			$\pm 0.1$	$\pm 1$	
$I_{OZ}$	$V_O = V_{CC}$ or GND, $V_I (\overline{OE}) = V_{IL}$ or $V_{IH}$	5.5 V				$\pm 0.25$	$\pm 2.5$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V				4	40	$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	5 V				2	10	pF
$C_o$	$V_O = V_{CC}$ or GND	5 V				3.5		pF



**SN74AHC244**  
**OCTAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A	Y	$C_L = 15\text{ pF}$	5.8	8.4	1	10	ns	
$t_{PHL}$				5.8	8.4	1	10		
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	6.6	10.6	1	12.5	ns	
$t_{PZL}$				6.6	10.6	1	12.5		
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	5	9.7	1	11	ns	
$t_{PLZ}$				5	9.7	1	11		
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$	8.3	11.9	1	13.5	ns	
$t_{PHL}$				8.3	11.9	1	13.5		
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	9.1	14.1	1	16	ns	
$t_{PZL}$				9.1	14.1	1	16		
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	10.3	14	1	16	ns	
$t_{PLZ}$				10.3	14	1	16		

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A	Y	$C_L = 15\text{ pF}$	3.9	5.5	1	6.5	ns	
$t_{PHL}$				3.9	5.5	1	6.5		
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	4.7	7.3	1	8.5	ns	
$t_{PZL}$				4.7	7.3	1	8.5		
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	5	7.2	1	8.5	ns	
$t_{PLZ}$				5	7.2	1	8.5		
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$	5.4	7.5	1	8.5	ns	
$t_{PHL}$				5.4	7.5	1	8.5		
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	6.2	9.3	1	10.5	ns	
$t_{PZL}$				6.2	9.3	1	10.5		
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	6.7	9.2	1	10.5	ns	
$t_{PLZ}$				6.7	9.2	1	10.5		

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER	$V_{CC}$	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_{sk(o)}$ Output skew	$3.3\text{ V} \pm 0.3\text{ V}$		1.5		1.5	ns
	$5\text{ V} \pm 0.5\text{ V}$		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.



# SN74AHC244 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

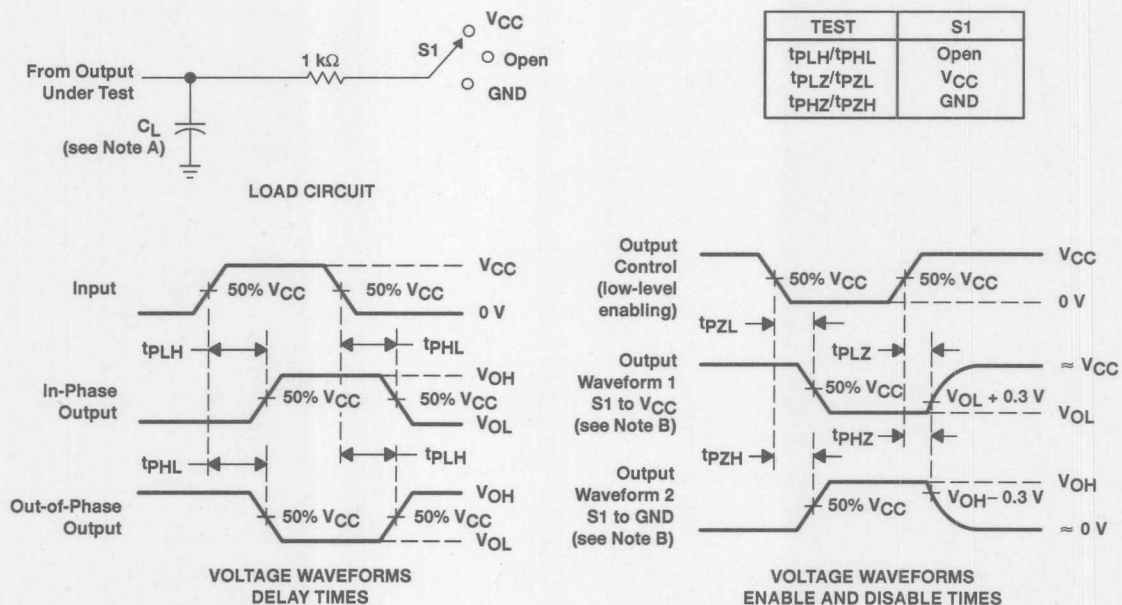
PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$		0.5		V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$		-0.2		V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		4.8		V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	8.6	pF

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OLP}$ Output output, maximum dynamic $V_{OL}$		0.5		V
$V_{OLM}$ Output output, minimum dynamic $V_{OL}$		-0.5		V
$V_{OHP}$ Output output, maximum dynamic $V_{OH}$		4.8		V
$V_{OHM}$ Output output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$ High-level dynamic input voltage	3.8			V
$V_{IL(D)}$ Low-level dynamic input voltage	1.5			V

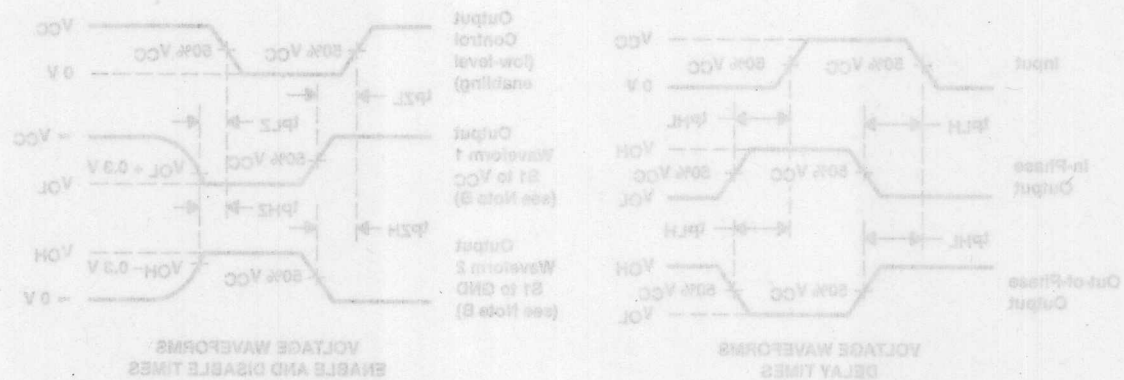
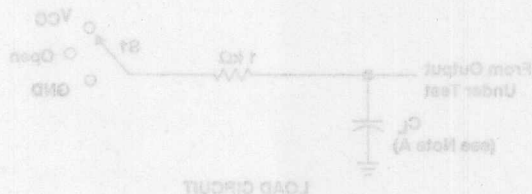
NOTE 5: Characteristics are determined during product characterization and are not for design purposes only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{PD}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	8.8	pF

## PARAMETER MEASUREMENT INFORMATION

TEST	SI
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are applied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $t_r \leq 20\text{ ns}$ ,  $t_f \leq 20\text{ ns}$ ,  $t_{d(1)} \leq 3\text{ ns}$ .  
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



# SN74AHC245 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCLS230A – OCTOBER 1995 – REVISED FEBRUARY 1995

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

## description

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

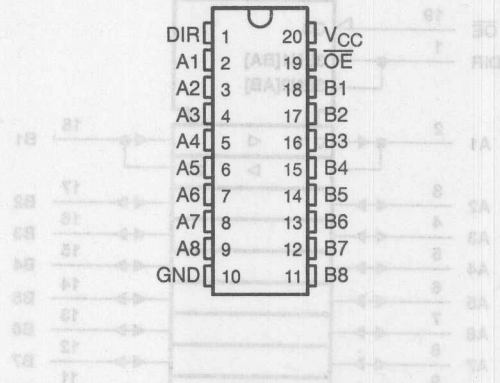
The SN74AHC245 allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

The SN74AHC245 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



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PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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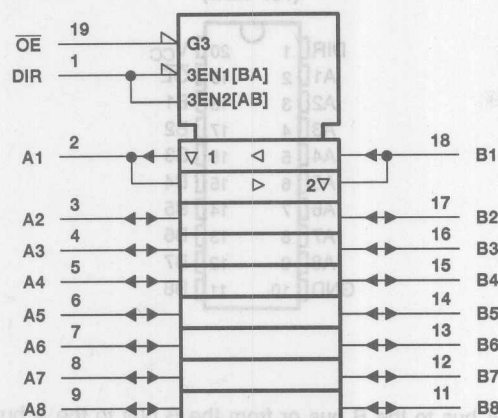
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# SN74AHC245

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

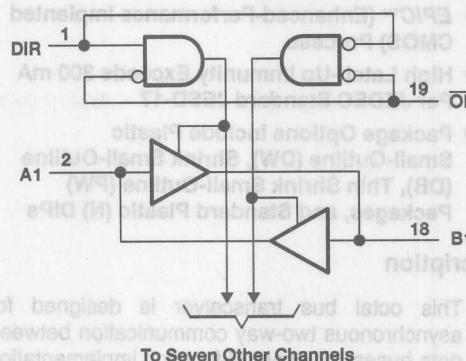
SCLS230A - OCTOBER 1995 - REVISED FEBRUARY 1995

### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	.....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	.....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	.....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	.....	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	.....	±25 mA
Continuous current through $V_{CC}$ or GND	.....	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):		
DB package	.....	0.6 W
DW package	.....	1.6 W
N package	.....	1.3 W
PW package	.....	0.7 W
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

# SN74AHC245 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 3 V	2.1		
		V <sub>CC</sub> = 5.5 V	3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5	V
		V <sub>CC</sub> = 3 V		0.9	
		V <sub>CC</sub> = 5.5 V		1.65	
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		-50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		-4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V		-8	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V		8	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V		100	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V		20	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
I <sub>I</sub>	A or B inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		±0.1		±1	μA
	$\overline{\text{OE}}$ or DIR				±0.1		±1	
I <sub>OZ</sub> <sup>†</sup>		V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> ( $\overline{\text{OE}}$ ) = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V		±0.25		±2.5	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		4		40	μA
C <sub>i</sub>	$\overline{\text{OE}}$ or DIR inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5	10		pF
C <sub>io</sub>	A or B inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4			pF

<sup>†</sup> The parameter I<sub>OZ</sub> includes the input leakage current.

**SN74AHC245**  
**OCTAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCLS230A – OCTOBER 1995 – REVISED FEBRUARY 1995

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A or B	B or A	$C_L = 15\text{ pF}$		5.8	8.4	1	10	ns
$t_{PHL}$					5.8	8.4	1	10	
$t_{PZH}$	$\overline{OE}$	A or B	$C_L = 15\text{ pF}$		8.5	13.2	1	15.5	ns
$t_{PZL}$					8.5	13.2	1	15.5	
$t_{PHZ}$	$\overline{OE}$	A or B	$C_L = 15\text{ pF}$		8.9	12.5	1	15.5	ns
$t_{PLZ}$					8.9	12.5	1	15.5	
$t_{PLH}$	A or B	B or A	$C_L = 50\text{ pF}$		8.3	11.9	1	13.5	ns
$t_{PHL}$					8.3	11.9	1	13.5	
$t_{PZH}$	$\overline{OE}$	A or B	$C_L = 50\text{ pF}$		11	16.7	1	19	ns
$t_{PZL}$					11	16.7	1	19	
$t_{PHZ}$	$\overline{OE}$	A or B	$C_L = 50\text{ pF}$		11.5	15.8	1	18	ns
$t_{PLZ}$					11.5	15.8	1	18	

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A or B	B or A	$C_L = 15\text{ pF}$		4	5.5	1	6.5	ns
$t_{PHL}$					4	5.5	1	6.5	
$t_{PZH}$	$\overline{OE}$	A or B	$C_L = 15\text{ pF}$		5.8	8.5	1	10	ns
$t_{PZL}$					5.8	8.5	1	10	
$t_{PHZ}$	$\overline{OE}$	A or B	$C_L = 15\text{ pF}$		5.6	7.8	1	9.2	ns
$t_{PLZ}$					5.6	7.8	1	9.2	
$t_{PLH}$	A or B	B or A	$C_L = 50\text{ pF}$		5.5	7.5	1	8.5	ns
$t_{PHL}$					5.5	7.5	1	8.5	
$t_{PZH}$	$\overline{OE}$	A or B	$C_L = 50\text{ pF}$		7.3	10.6	1	12	ns
$t_{PZL}$					7.3	10.6	1	12	
$t_{PHZ}$	$\overline{OE}$	A or B	$C_L = 50\text{ pF}$		7	9.7	1	11	ns
$t_{PLZ}$					7	9.7	1	11	

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER		$V_{CC}$	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
$t_{sk(o)}$	Output skew	$3.3\text{ V} \pm 0.3\text{ V}$		1.5		1.5	ns
		$5\text{ V} \pm 0.5\text{ V}$		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.





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## OCTAL BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

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noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

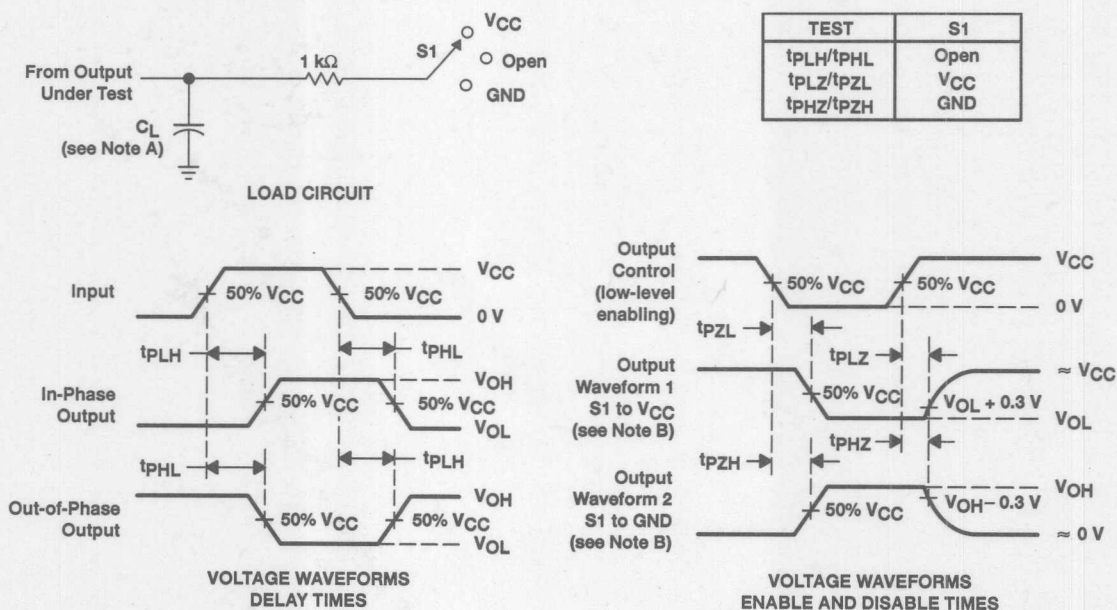
PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$		0.9		V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$		-0.9		V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		4.3		V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per transceiver	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	14	pF

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OLP}$ Quiet output, maximum dynamic $V_{OL}$		0.9		V
$V_{OLM}$ Quiet output, minimum dynamic $V_{OL}$		-0.8		V
$V_{OHM}$ Quiet output, minimum dynamic $V_{OH}$		4.3		V
$V_{OHV}$ Quiet output, maximum dynamic $V_{OH}$		3.5		V
High-level dynamic input voltage			1.8	V
Low-level dynamic input voltage			1.8	V

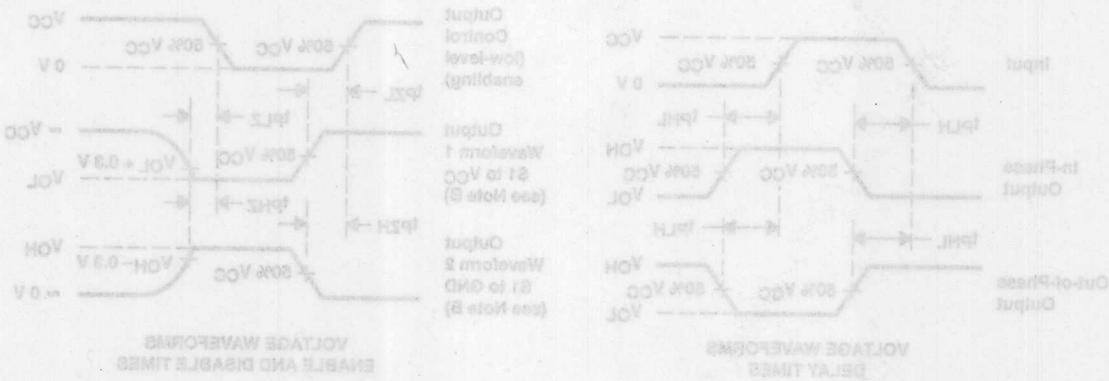
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per transceiver	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	14	pF

# PARAMETER MEASUREMENT INFORMATION

TEST	SI
PRH/PHL	Open
PLZ/PLZ	$V_{CC}$
PHZ/PHZ	GND



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is low except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz,  $t_r = 2\text{ ns}$ ,  $t_f = 2\text{ ns}$ .  
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# SN74AHC373

## OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

### description

The SN74AHC373 is an octal transparent D-type latch.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

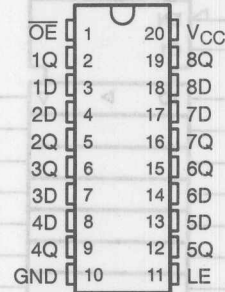
$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHC373 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



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**TEXAS  
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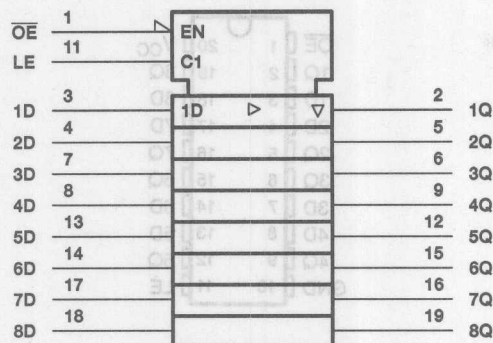
# SN74AHC373

## OCTAL TRANSPARENT D-TYPE LATCH

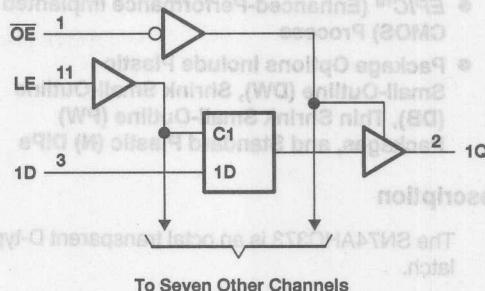
### WITH 3-STATE OUTPUTS

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#### logic symbol†



#### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	

DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W

Storage temperature range, $T_{stg}$	-65°C to 150°C
--------------------------------------	----------------

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

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**OCTAL TRANSPARENT D-TYPE LATCH**  
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recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		V
		$V_{CC} = 3\text{ V}$	2.1		
		$V_{CC} = 5.5\text{ V}$	3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5	V
		$V_{CC} = 3\text{ V}$		0.9	
		$V_{CC} = 5.5\text{ V}$		1.65	
$V_I$	Input voltage		0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$		-50	$\mu\text{A}$
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		-4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		-8	
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$		50	$\mu\text{A}$
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		20	
$T_A$	Operating free-air temperature		-40	85	$^{\circ}\text{C}$

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^{\circ}\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50\text{ }\mu\text{A}$	2 V	1.9			1.9		V
		3 V	2.9			2.9		
		4.5 V	4.4			4.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		
	$I_{OH} = -8\text{ mA}$	4.5 V	3.94			3.8		
$V_{OL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	$I_{OL} = 4\text{ mA}$	3 V			0.36		0.44	
	$I_{OL} = 8\text{ mA}$	4.5 V			0.36		0.44	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$	$\mu\text{A}$
$I_{OZ}$	$V_I = V_{IH}$ or $V_{IL}$ , $V_O = V_{CC}$ or GND	5.5 V			$\pm 0.25$		$\pm 2.5$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40	$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF
$C_o$		5 V		6				pF

PRODUCT PREVIEW



# SN74AHC373 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCLS235 – OCTOBER 1995

timing requirements over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_W$	Pulse duration, $\overline{LE}$ high	5		5		ns
$t_{SU}$	Setup time, data before $\overline{LE}\downarrow$	4		4		ns
$t_H$	Hold time, data after $\overline{LE}\downarrow$	1		1		ns

timing requirements over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_W$	Pulse duration, $\overline{LE}$ high	5		5		ns
$t_{SU}$	Setup time, data before $\overline{LE}\downarrow$	4		4		ns
$t_H$	Hold time, data after $\overline{LE}\downarrow$	1		1		ns

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 15 pF	7.3	11.4	1	13.5	ns	
t <sub>PHL</sub>				7.3	11.4	1	13.5		
t <sub>PLH</sub>	LE	Q		7	11	1	13	ns	
t <sub>PHL</sub>				7	11	1	13		
t <sub>PZH</sub>	OE	Q		7.3	11.4	1	13.5	ns	
t <sub>PZL</sub>				7.3	11.4	1	13.5		
t <sub>PHZ</sub>	OE	Q						ns	
t <sub>PLZ</sub>									
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 50 pF	9.8	14.9	1	17	ns	
t <sub>PHL</sub>				9.8	14.9	1	17		
t <sub>PLH</sub>	LE	Q		9.5	14.5	1	16.5	ns	
t <sub>PHL</sub>				9.5	14.5	1	16.5		
t <sub>PZH</sub>	OE	Q		9.8	14.9	1	17	ns	
t <sub>PZL</sub>				9.8	14.9	1	17		
t <sub>PHZ</sub>	OE	Q		9.5	13.2	1	15	ns	
t <sub>PLZ</sub>				9.5	13.2	1	15		

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**SN74AHC373**  
**OCTAL TRANSPARENT D-TYPE LATCH**  
**WITH 3-STATE OUTPUTS**  
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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 15 pF	5	7.2	1	8.5	ns	
t <sub>PHL</sub>				5	7.2	1	8.5		
t <sub>PLH</sub>	LE	Q		4.9	7.2	1	8.5	ns	
t <sub>PHL</sub>				4.9	7.2	1	8.5		
t <sub>PZH</sub>	$\overline{OE}$	Q		5.5	8.1	1	9.5	ns	
t <sub>PZL</sub>				5.5	8.1	1	9.5		
t <sub>PHZ</sub>	$\overline{OE}$	Q						ns	
t <sub>PLZ</sub>									
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 50 pF	6.5	9.2	1	10.5	ns	
t <sub>PHL</sub>				6.5	9.2	1	10.5		
t <sub>PLH</sub>	LE	Q		6.4	9.2	1	10.5	ns	
t <sub>PHL</sub>				6.4	9.2	1	10.5		
t <sub>PZH</sub>	$\overline{OE}$	Q		7	10.1	1	11.5	ns	
t <sub>PZL</sub>				7	10.1	1	11.5		
t <sub>PHZ</sub>	$\overline{OE}$	Q		6.5	9.2	1	10.5	ns	
t <sub>PLZ</sub>				6.5	9.2	1	10.5		

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER	$V_{CC}$	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_{sk(o)}$ Output skew	$3.3\text{ V} \pm 0.3\text{ V}$		1.5		1.5	ns
	$5\text{ V} \pm 0.5\text{ V}$		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$		27		pF

PRODUCT PREVIEW



# SN74AHC373 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCLS235 - OCTOBER 1995

## PARAMETER MEASUREMENT INFORMATION

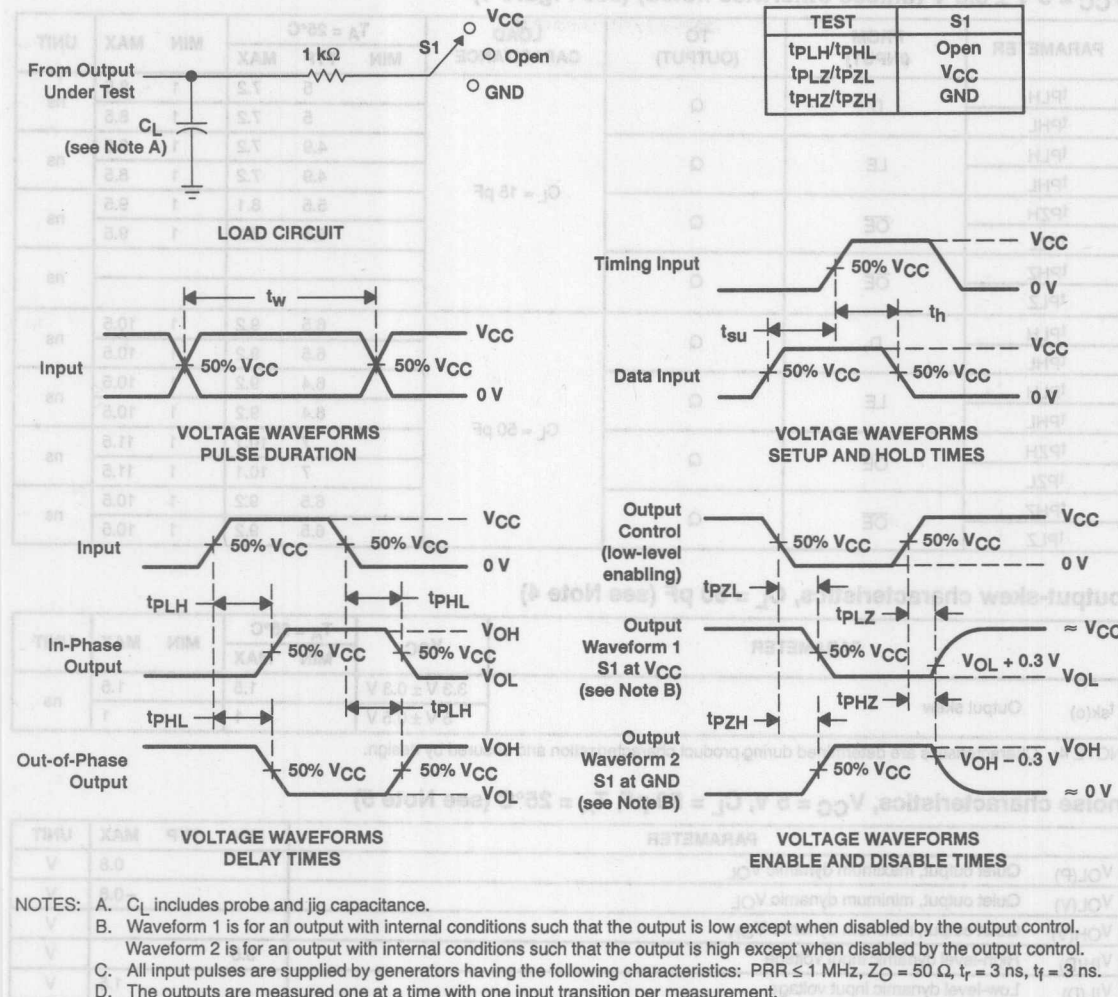


Figure 1. Load Circuit and Voltage Waveforms

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power dissipation capacitance	$C_L = 50 \text{ pF}$ , $f = 1 \text{ MHz}$		37		pF

# SN74AHC374

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCLS240 – OCTOBER 1995

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- 3-State Outputs Drive Bus Lines Directly
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

### description

The SN74AHC374 is an octal edge-triggered D-type flip-flop that features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

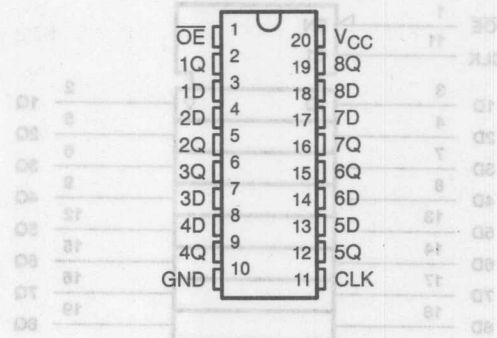
On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHC374 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	$\uparrow$	H or L	X
H	X	X	Z

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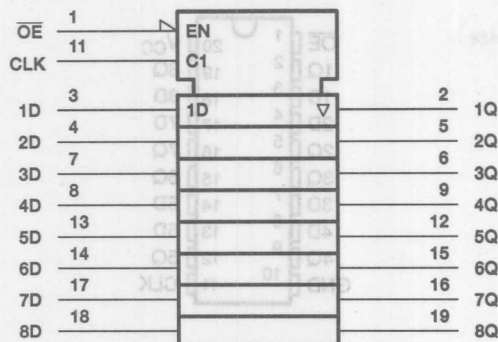
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# SN74AHC374

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

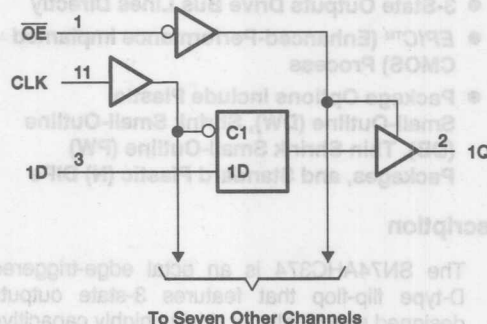
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### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

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recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		
		$V_{CC} = 3\text{ V}$	2.1		V
		$V_{CC} = 5.5\text{ V}$	3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5	
		$V_{CC} = 3\text{ V}$		0.9	V
		$V_{CC} = 5.5\text{ V}$		1.65	
$V_I$	Input voltage		0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$		-50	$\mu\text{A}$
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		-4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		-8	
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$		50	$\mu\text{A}$
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		20	
$T_A$	Operating free-air temperature		-40	85	$^{\circ}\text{C}$

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^{\circ}\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50\text{ }\mu\text{A}$	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
$V_{OL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	$I_{OL} = 4\text{ mA}$	3 V			0.36		0.44	
		4.5 V			0.36		0.44	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$	$\mu\text{A}$
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.5 V			$\pm 0.25$		$\pm 2.5$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40	$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	5 V		4	10			pF
$C_o$	$V_O = V_{CC}$ or GND	5 V		6				pF

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timing requirements over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_w$	Pulse duration, CLK high or low	5		5.5		ns
$t_{su}$	Setup time, data before CLK $\uparrow$	4.5		4		ns
$t_h$	Hold time, data after CLK $\uparrow$	2		2		ns

timing requirements over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_w$	Pulse duration, CLK high or low	5		5		ns
$t_{su}$	Setup time, data before CLK $\uparrow$	3		3		ns
$t_h$	Hold time, data after CLK $\uparrow$	2		2		ns

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f <sub>max</sub>			C <sub>L</sub> = 15 pF	80	130		70		MHz
			C <sub>L</sub> = 50 pF	55	85		50		
t <sub>PLH</sub>	CLK	Q	C <sub>L</sub> = 15 pF	8.1	12.7		1	15	ns
t <sub>PHL</sub>				8.1	12.7		1	15	
t <sub>PZH</sub>	OE	Q		7.1	11		1	13	ns
t <sub>PZL</sub>				7.1	11		1	13	
t <sub>PHZ</sub>	OE	Q							ns
t <sub>PLZ</sub>									
t <sub>PLH</sub>	CLK	Q	C <sub>L</sub> = 50 pF	10.6	16.2		1	18.5	ns
t <sub>PHL</sub>				10.6	16.2		1	18.5	
t <sub>PZH</sub>	OE	Q		9.6	14.5		1	16.5	ns
t <sub>PZL</sub>				9.6	14.5		1	16.5	
t <sub>PHZ</sub>	OE	Q		10.2	14		1	16	ns
t <sub>PLZ</sub>				10.2	14		1	16	

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**OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP**  
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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f <sub>max</sub>			C <sub>L</sub> = 15 pF	130	185		110		MHz
			C <sub>L</sub> = 50 pF	85	120		75		
t <sub>PLH</sub>	CLK	Q	C <sub>L</sub> = 15 pF		5.4	8.1	1	9.5	ns
t <sub>PHL</sub>					5.4	8.1	1	9.5	
t <sub>PZH</sub>	OE	Q			5.1	7.6	1	9	ns
t <sub>PZL</sub>					5.1	7.6	1	9	
t <sub>PHZ</sub>	OE	Q							ns
t <sub>PLZ</sub>									
t <sub>PLH</sub>	CLK	Q	C <sub>L</sub> = 50 pF		6.9	10.1	1	11.5	ns
t <sub>PHL</sub>					6.9	10.1	1	11.5	
t <sub>PZH</sub>	OE	Q			6.6	9.6	1	11	ns
t <sub>PZL</sub>					6.6	9.6	1	11	
t <sub>PHZ</sub>	OE	Q			6.1	8.8	1	10	ns
t <sub>PLZ</sub>					6.1	8.8	1	10	

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER	$V_{CC}$	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_{\text{sk(o)}}$ Output skew	$3.3\text{ V} \pm 0.3\text{ V}$		1.5		1.5	ns
	$5\text{ V} \pm 0.5\text{ V}$		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

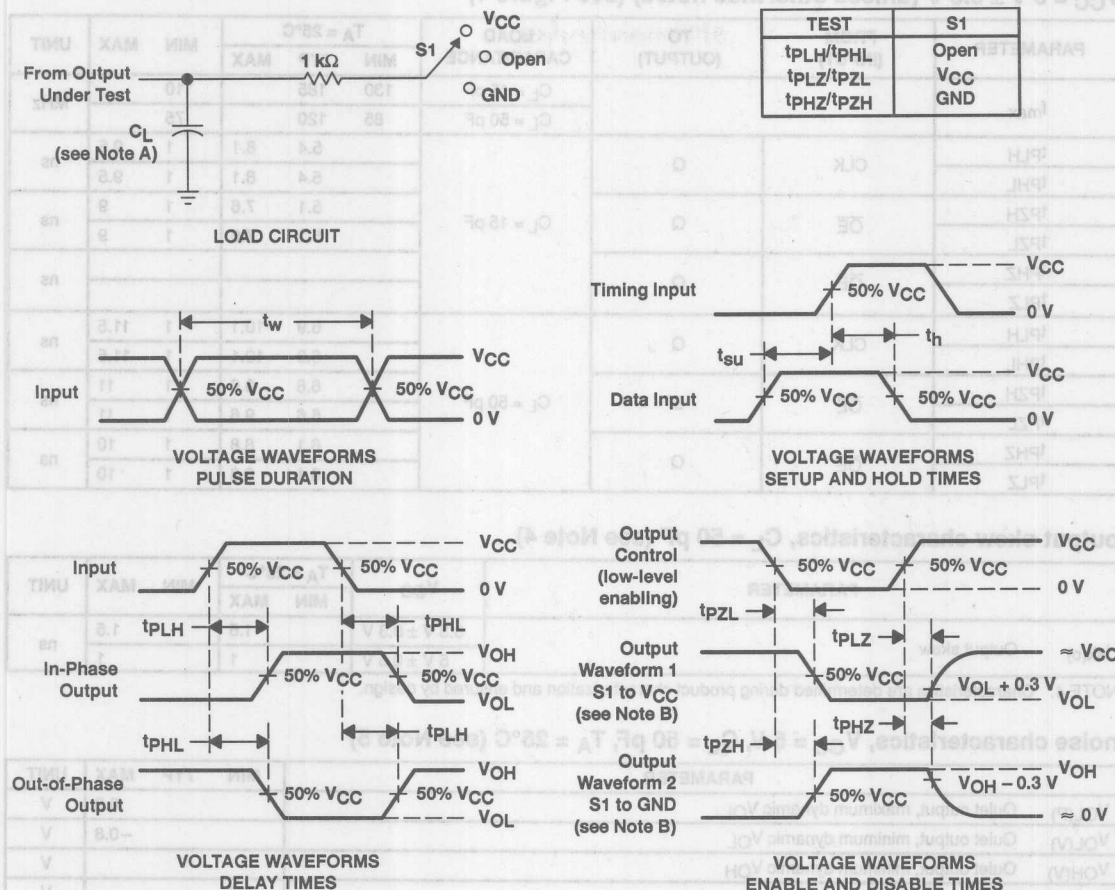
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{\text{pd}}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$		32		pF

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub> = 3 ns, t<sub>f</sub> = 3 ns.
  - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# SN74AHC540 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

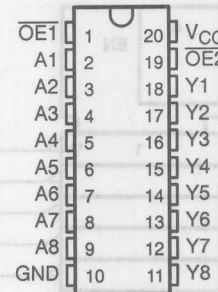
## description

The SN74AHC540 octal buffer/driver is ideal for driving bus lines or buffer memory address registers. This device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

The SN74AHC540 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

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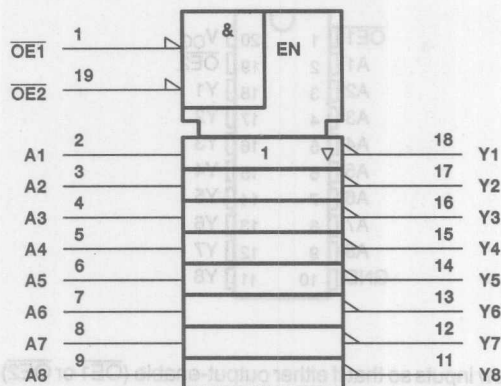
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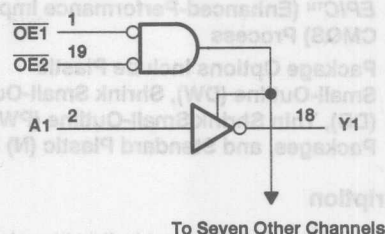
**SN74AHC540**  
**OCTAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**  
 SCLS260 – DECEMBER 1995

**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**logic diagram (positive logic)**



To Seven Other Channels

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

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**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	V
		V <sub>CC</sub> = 3 V	2.1	
		V <sub>CC</sub> = 5.5 V	3.85	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	V
		V <sub>CC</sub> = 3 V	0.9	
		V <sub>CC</sub> = 5.5 V	1.65	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	– 50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V	– 4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V	– 8	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V	4	mA
		V <sub>CC</sub> = 5 V ± 0.5 V	8	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V	100	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V	20	
T <sub>A</sub>	Operating free-air temperature	– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = – 50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = – 4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = – 8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
I <sub>I</sub>	Data inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		± 0.1		± 1	μA
	Control inputs				± 0.1		± 1	
I <sub>OZ</sub> <sup>†</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> (OE) = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V			± 0.25		± 2.5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10		10	pF
C <sub>o</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		6				pF

<sup>†</sup> For I/O pins, the parameter I<sub>OZ</sub> includes the input leakage current.

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# SN74AHC540

## OCTAL BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	4.8	7	1	8.5	ns	
t <sub>PHL</sub>		Y		4.8	7	1	8.5		
t <sub>PZH</sub>	OE	Y		6.8	10.5	1	12.5	ns	
t <sub>PZL</sub>		Y		6.8	10.5	1	12.5		
t <sub>PHZ</sub>	OE	Y						ns	
t <sub>PLZ</sub>		Y							
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	7.3	10.5	1	12	ns	
t <sub>PHL</sub>		Y		7.3	10.5	1	12		
t <sub>PZH</sub>	OE	Y		9.3	14	1	16	ns	
t <sub>PZL</sub>		Y		9.3	14	1	16		
t <sub>PHZ</sub>	OE	Y		11.2	15.4	1	17.5	ns	
t <sub>PLZ</sub>		Y		11.2	15.4	1	17.5		

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

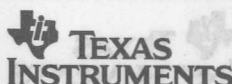
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	3.7	5	1	6	ns	
t <sub>PHL</sub>				3.7	5	1	6		
t <sub>PZH</sub>	OE	Y		4.7	7.2	1	8.5	ns	
t <sub>PZL</sub>				4.7	7.2	1	8.5		
t <sub>PHZ</sub>	OE	Y						ns	
t <sub>PLZ</sub>									
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	5.2	7	1	8	ns	
t <sub>PHL</sub>				5.2	7	1	8		
t <sub>PZH</sub>	OE	Y		6.2	9.2	1	10.5	ns	
t <sub>PZL</sub>				6.2	9.2	1	10.5		
t <sub>PHZ</sub>	OE	Y		6	8.8	1	10	ns	
t <sub>PLZ</sub>				6	8.8	1	10		

output-skew characteristics,  $C_L = 50 \text{ pF}$  (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	$3.3 \text{ V} \pm 0.3 \text{ V}$			1.5		1.5	ns
			$5 \text{ V} \pm 0.5 \text{ V}$			1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

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noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

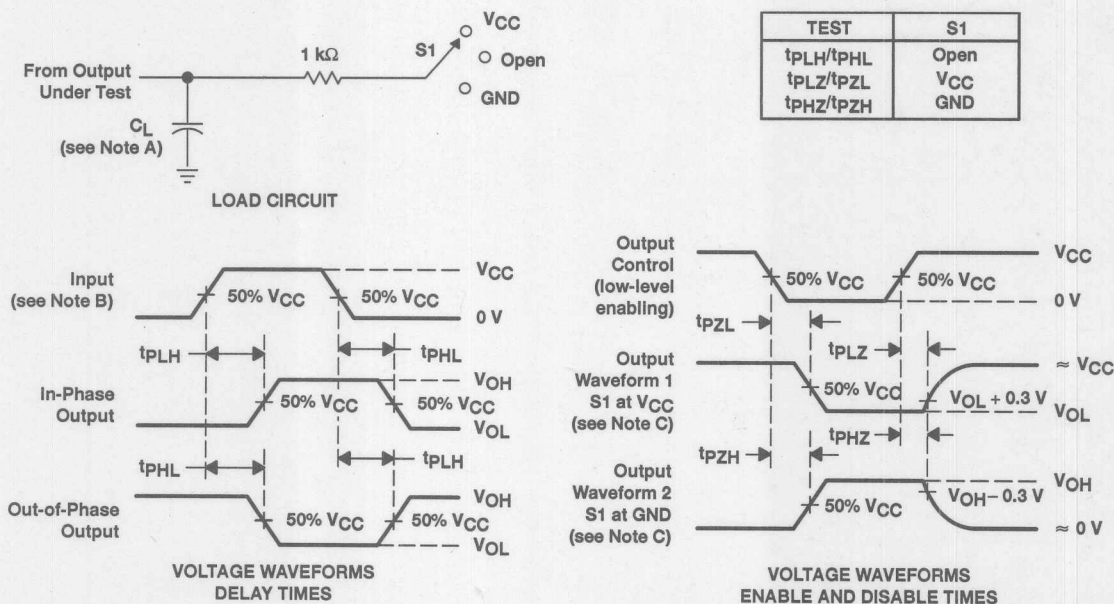
PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage		1.5		V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$				pF

### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OLP}$ (1)			0.8	V
$V_{OLN}$ (2)			-0.8	V
$V_{OHP}$ (3)				V
$V_{OHN}$ (4)				V
$V_{IH(1)}$	3.5			V
$V_{IL(1)}$	1.5			V

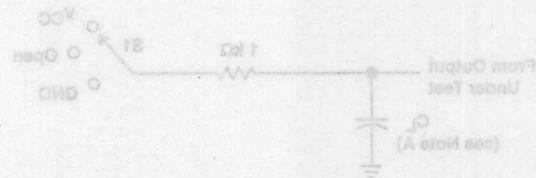
NOTE 5: Characteristics are determined during product characterization and entered by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

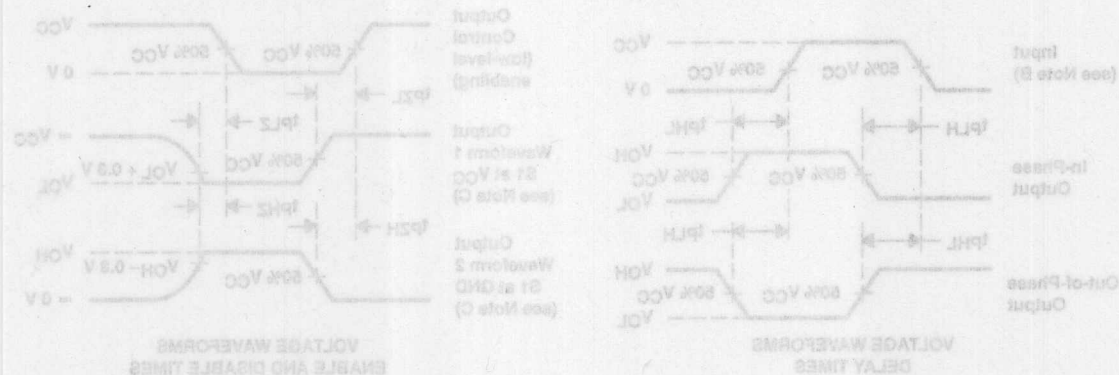
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{pd}$	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$				pF

# PARAMETER MEASUREMENT INFORMATION

TEST	SI
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PLZ}$ , $t_{PHZ}$	$V_{CC}$
$t_{PHZ}$ , $t_{PLZ}$	GND



LOAD CIRCUIT



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
D. The outputs are measured one at a time with one input variation per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

# SN74AHC541 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCLS261B – DECEMBER 1995 – REVISED JANUARY 1996

- Operating Range: 2-V to 5.5-V  $V_{CC}$
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

## description

The SN74AHC541 octal buffer/driver is ideal for driving bus lines or buffer memory address registers. This device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

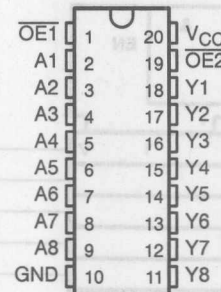
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

The SN74AHC541 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



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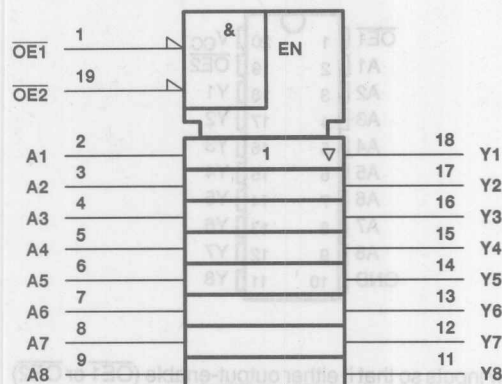
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# SN74AHC541 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

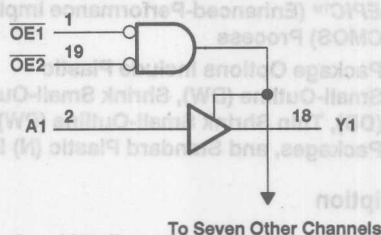
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



To Seven Other Channels

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW



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# SN74AHC541 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 3 V	2.1		
		V <sub>CC</sub> = 5.5 V	3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5	V
		V <sub>CC</sub> = 3 V		0.9	
		V <sub>CC</sub> = 5.5 V		1.65	
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		– 50	μA
		V <sub>CC</sub> = 3.3 ± 0.3 V		– 4	mA
		V <sub>CC</sub> = 5 ± 0.5 V		– 8	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	μA
		V <sub>CC</sub> = 3.3 ± 0.3 V		4	mA
		V <sub>CC</sub> = 5 ± 0.5 V		8	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 ± 0.3 V		100	ns/V
		V <sub>CC</sub> = 5 ± 0.5 V		20	
T <sub>A</sub>	Operating free-air temperature		– 40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = – 50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = – 4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = – 8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
I <sub>I</sub>	Data inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		± 0.1		± 1	μA
	Control inputs				± 0.1		± 1	
I <sub>OZ</sub> <sup>†</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> (OE) = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V			± 0.25		± 2.5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			4	10	10	pF
C <sub>o</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			6			pF

<sup>†</sup> For input and output, I<sub>OZ</sub> includes the input leakage current.

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PRODUCT PREVIEW

# **SN74AHC541** **OCTAL BUFFER/DRIVER** **WITH 3-STATE OUTPUTS**

SCLS261B – DECEMBER 1995 – REVISED JANUARY 1996

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	5	7	1	8.5	ns	
t <sub>PHL</sub>				5	7	1	8.5		
t <sub>PZH</sub>	OE	Y		6.8	10.5	1	12.5	ns	
t <sub>PZL</sub>				6.8	10.5	1	12.5		
t <sub>PHZ</sub>	OE	Y						ns	
t <sub>PLZ</sub>									
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	7.5	10.5	1	12	ns	
t <sub>PHL</sub>				7.5	10.5	1	12		
t <sub>PZH</sub>	OE	Y		9.3	14	1	16	ns	
t <sub>PZL</sub>				9.3	14	1	16		
t <sub>PHZ</sub>	OE	Y		11.2	15.4	1	17.5	ns	
t <sub>PLZ</sub>				11.2	15.4	1	17.5		

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF		3.5	5	1	6	ns
t <sub>PHL</sub>					3.5	5	1	6	
t <sub>PZH</sub>	OE	Y			4.7	7.2	1	8.5	ns
t <sub>PZL</sub>					4.7	7.2	1	8.5	
t <sub>PHZ</sub>	OE	Y							ns
t <sub>PLZ</sub>									
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF		5	7	1	8	ns
t <sub>PHL</sub>					5	7	1	8	
t <sub>PZH</sub>	OE	Y			6.2	9.2	1	10.5	ns
t <sub>PZL</sub>					6.2	9.2	1	10.5	
t <sub>PHZ</sub>	OE	Y			6	8.8	1	10	ns
t <sub>PLZ</sub>					6	8.8	1	10	

output-skew characteristics,  $C_L = 50 \text{ pF}$  (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	$3.3 \text{ V} \pm 0.3 \text{ V}$			1.5		1.5	ns
			$5 \text{ V} \pm 0.5 \text{ V}$			1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

PRODUCT PREVIEW



# SN74AHC541 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCLS261B – DECEMBER 1995 – REVISED JANUARY 1996

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

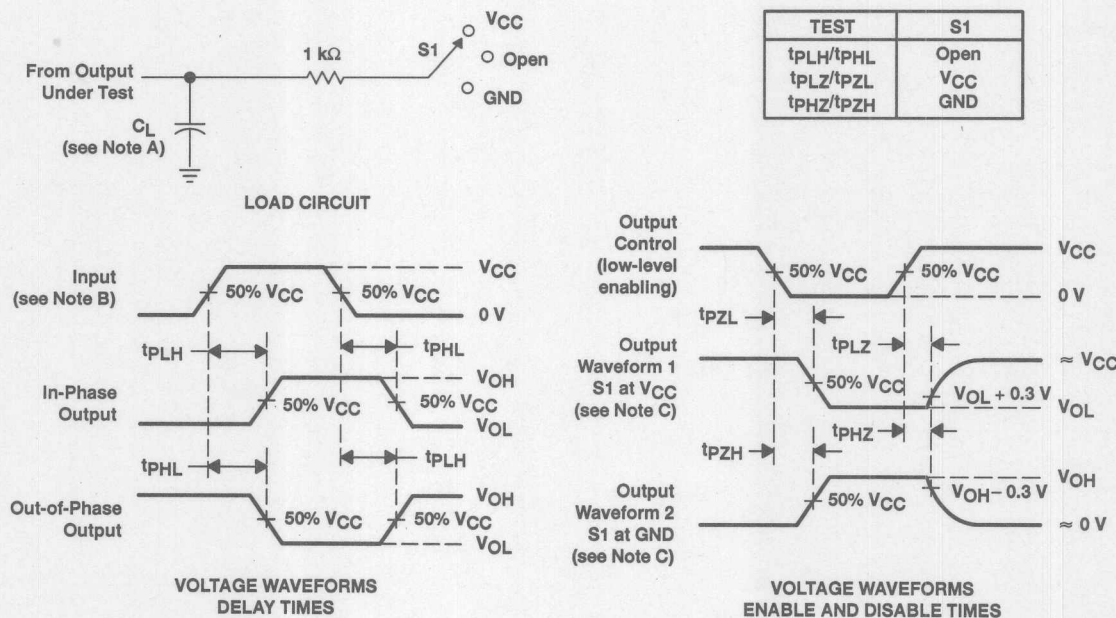
PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage		1.5		V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$		pF

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 80\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OLP}$ Output output, maximum dynamic $V_{OL}$			0.8	V
$V_{OLM}$ Output output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OHV}$ Output output, minimum dynamic $V_{OH}$				V
$V_{OHV}$ High-level dynamic input voltage	2.5			V
$V_{ILD}$ Low-level dynamic input voltage	1.5			V

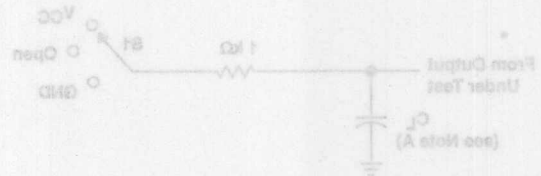
NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

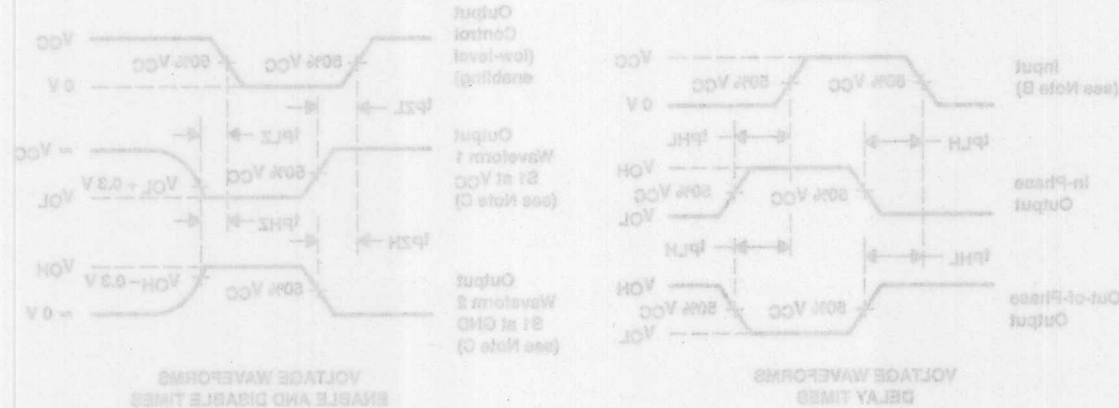
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 80\text{ pF}$ , $f = 1\text{ MHz}$		pF

# PARAMETER MEASUREMENT INFORMATION

TEST	SI
1P1H/1P1L	Open
1P1Z/1P2L	$V_{CC}$
1P1Z/1P2H	GND



LOAD CIRCUIT



NOTE: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_0 = 50\text{ }\Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



# SN74AHC573 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCLS242B – OCTOBER 1995 – REVISED JANUARY 1996

- 3-State Outputs Directly Drive Bus Lines
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

## description

The SN74AHC573 is an octal transparent D-type latch.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

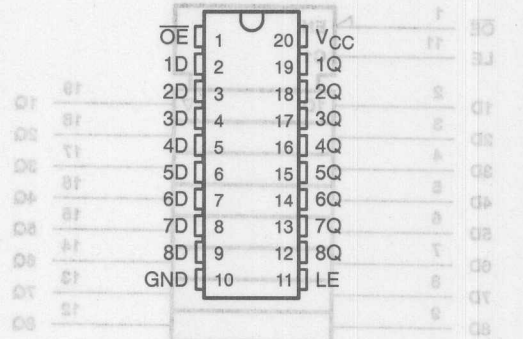
$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHC573 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

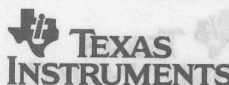
DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



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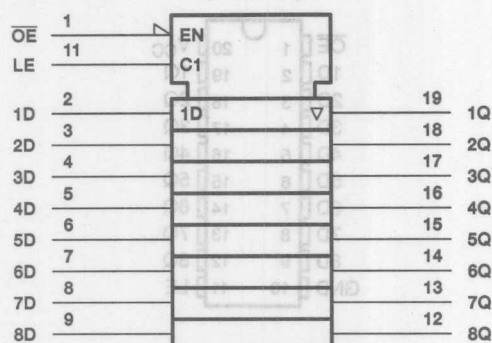
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# SN74AHC573

## OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

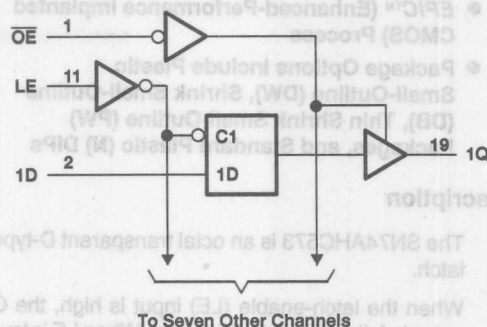
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### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



To Seven Other Channels

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW



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**SN74AHC573**  
**OCTAL TRANSPARENT D-TYPE LATCH**  
**WITH 3-STATE OUTPUTS**

SCLS242B – OCTOBER 1995 – REVISED JANUARY 1996

**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V 1.5 V <sub>CC</sub> = 3 V 2.1 V <sub>CC</sub> = 5.5 V 3.85		V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V 0.5 V <sub>CC</sub> = 3 V 0.9 V <sub>CC</sub> = 5.5 V 1.65		V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V -50 V <sub>CC</sub> = 3.3 V ± 0.3 V -4 V <sub>CC</sub> = 5 V ± 0.5 V -8		μA mA
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V 50 V <sub>CC</sub> = 3.3 V ± 0.3 V 8 V <sub>CC</sub> = 5 V ± 0.5 V 4		μA mA
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V 100 V <sub>CC</sub> = 5 V ± 0.5 V 20		ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
		4.5 V			0.36		0.44	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	μA
I <sub>OZ</sub>	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub> , V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		2.5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	μA
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10		10	pF
C <sub>O</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		6				

PRODUCT PREVIEW



# SN74AHC573 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCLS242B – OCTOBER 1995 – REVISED JANUARY 1996

timing requirements over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_W$	Pulse duration, $\overline{LE}$ high	5		5		ns
$t_{su}$	Setup time, data before $\overline{LE}\downarrow$	3.5		3.5		ns
$t_h$	Hold time, data after $\overline{LE}\downarrow$	1.5		1.5		ns

timing requirements over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_W$	Pulse duration, $\overline{LE}$ high	5		5		ns
$t_{su}$	Setup time, data before $\overline{LE}\downarrow$	3.5		3.5		ns
$t_h$	Hold time, data after $\overline{LE}\downarrow$	1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 15 pF	7	11	1	13	ns	
t <sub>PHL</sub>				7	11	1	13		
t <sub>PLH</sub>	LE	Q		7.6	11.9	1	14	ns	
t <sub>PHL</sub>				7.6	11.9	1	14		
t <sub>PZH</sub>	OE	Q		7.3	11.5	1	13.5	ns	
t <sub>PZL</sub>				7.3	11.5	1	13.5		
t <sub>PHZ</sub>	OE	Q						ns	
t <sub>PLZ</sub>									
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 50 pF	9.5	14.5	1	16.5	ns	
t <sub>PHL</sub>				9.5	14.5	1	16.5		
t <sub>PLH</sub>	LE	Q		10.1	15.4	1	17.5	ns	
t <sub>PHL</sub>				10.1	15.4	1	17.5		
t <sub>PZH</sub>	OE	Q		9.8	15	1	17	ns	
t <sub>PZL</sub>				9.8	15	1	17		
t <sub>PHZ</sub>	OE	Q		10.7	14.5	1	16.5	ns	
t <sub>PLZ</sub>				10.7	14.5	1	16.5		

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**SN74AHC573**  
**OCTAL TRANSPARENT D-TYPE LATCH**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 15 pF	4.5	6.8	1	8	ns	
t <sub>PHL</sub>				4.5	6.8	1	8		
t <sub>PLH</sub>	LE	Q		5	7.7	1	9	ns	
t <sub>PHL</sub>				5	7.7	1	9		
t <sub>PZH</sub>	OE	Q		5.2	7.7	1	9	ns	
t <sub>PZL</sub>				5.2	7.7	1	9		
t <sub>PHZ</sub>	OE	Q						ns	
t <sub>PLZ</sub>									
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 50 pF	6	8.8	1	10	ns	
t <sub>PHL</sub>				6	8.8	1	10		
t <sub>PLH</sub>	LE	Q		6.5	9.7	1	11	ns	
t <sub>PHL</sub>				6.5	9.7	1	11		
t <sub>PZH</sub>	OE	Q		6.7	9.7	1	11	ns	
t <sub>PZL</sub>				6.7	9.7	1	11		
t <sub>PHZ</sub>	OE	Q		6.7	9.7	1	11	ns	
t <sub>PLZ</sub>				6.7	9.7	1	11		

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER	$V_{CC}$	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_{sk(o)}$ Output skew	$3.3\text{ V} \pm 0.3\text{ V}$		1.5		1.5	ns
	$5\text{ V} \pm 0.5\text{ V}$		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design and for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	29	pF

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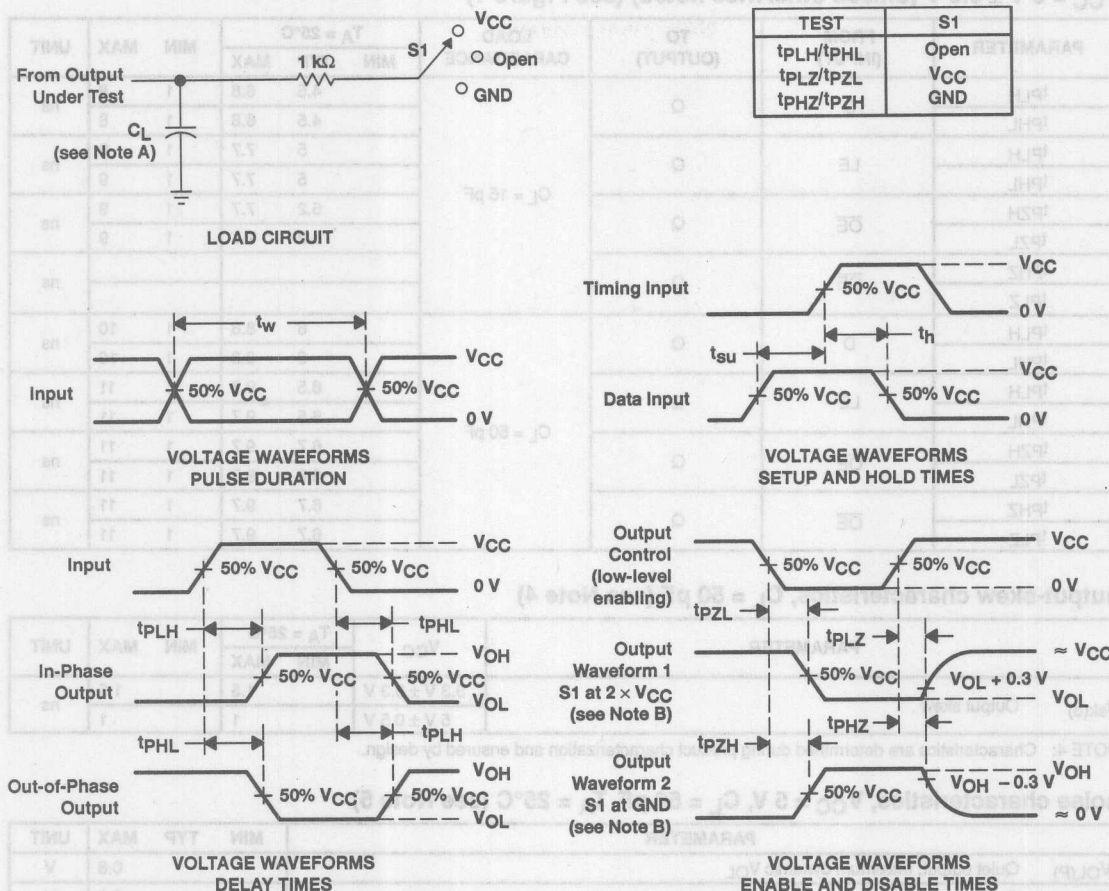




# SN74AHC573 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER	TEST CONDITIONS	UNIT
Power dissipation	$C_L = 50$ pF, $f = 1$ MHz	W



# SN74AHC574

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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- Operating Range: 2-V to 5.5-V  $V_{CC}$
- 3-State Outputs Directly Drive Bus Lines
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

### description

The SN74AHC574 is an octal edge-triggered D-type flip-flop that features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

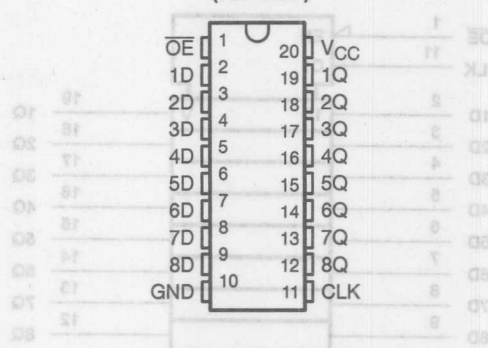
On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHC574 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	$Q_0$
H	X	X	Z

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**TEXAS  
INSTRUMENTS**

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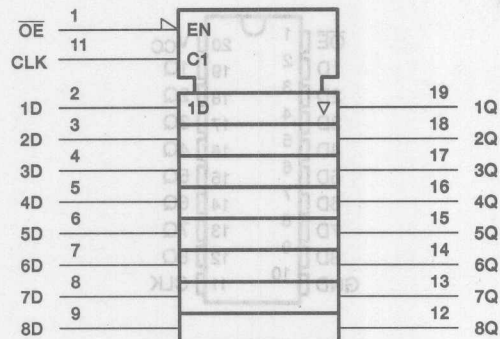
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# **SN74AHC574** **OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP** **WITH 3-STATE OUTPUTS**

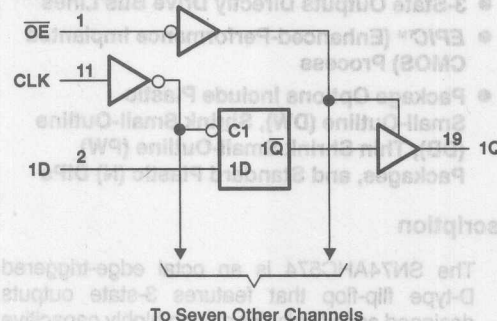
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## **logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## **logic diagram (positive logic)**



## **absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

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# SN74AHC574

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP

### WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

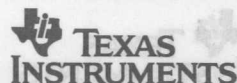
		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$ 1.5 $V_{CC} = 3\text{ V}$ 2.1 $V_{CC} = 5.5\text{ V}$ 3.85		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$ 0.5 $V_{CC} = 3\text{ V}$ 0.9 $V_{CC} = 5.5\text{ V}$ 1.65		V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$ -50 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ -4 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ -8		$\mu\text{A}$ mA
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$ 50 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ 4 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ 8		$\mu\text{A}$ mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ 100 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ 20		ns/V
$T_A$	Operating free-air temperature	-40	85	$^{\circ}\text{C}$

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^{\circ}\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50\text{ }\mu\text{A}$	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		
	$I_{OH} = -8\text{ mA}$	4.5 V	3.94			3.8		
$V_{OL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	$I_{OL} = 4\text{ mA}$	3 V			0.36		0.44	
	$I_{OL} = 8\text{ mA}$	4.5 V			0.36		0.44	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$	$\mu\text{A}$
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.5 V			$\pm 0.25$		$\pm 2.5$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40	$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	5 V			4	10	10	pF
$C_o$	$V_O = V_{CC}$ or GND	5 V			6			pF

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# **SN74AHC574** **OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP** **WITH 3-STATE OUTPUTS**

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**timing requirements over recommended operating free-air temperature range,**  
 **$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)**

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_W$	Pulse duration, CLK high or low	5		5.5		ns
$t_{SU}$	Setup time, data before CLK $\uparrow$	3.5		3.5		ns
$t_H$	Hold time, data after CLK $\uparrow$	1.5		1.5		ns

**timing requirements over recommended operating free-air temperature range,**  
 **$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)**

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_W$	Pulse duration, CLK high or low	5		5		ns
$t_{SU}$	Setup time, data before CLK $\uparrow$	3.5		3.5		ns
$t_H$	Hold time, data after CLK $\uparrow$	1.5		1.5		ns

**switching characteristics over recommended operating free-air temperature range,**  
 **$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f <sub>max</sub>			C <sub>L</sub> = 15 pF	80	125		65		MHz
			C <sub>L</sub> = 50 pF	50	75		45		
t <sub>PLH</sub>	CLK	Q	C <sub>L</sub> = 15 pF	8.5	13.2		1	15.5	ns
t <sub>PHL</sub>				8.5	13.2		1	15.5	
t <sub>PZH</sub>	OE	Q		8.2	12.8		1	15	ns
t <sub>PZL</sub>				8.2	12.8		1	15	
t <sub>PHZ</sub>	OE	Q	C <sub>L</sub> = 50 pF						ns
t <sub>PLZ</sub>									
t <sub>PLH</sub>	CLK	Q		11	16.7		1	19	ns
t <sub>PHL</sub>				11	16.7		1	19	
t <sub>PZH</sub>	OE	Q		10.7	16.3		1	18.5	ns
t <sub>PZL</sub>				10.7	16.3		1	18.5	
t <sub>PHZ</sub>	OE	Q		11	15		1	17	ns
t <sub>PLZ</sub>				11	15		1	17	

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**SN74AHC574**  
**OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**  
SCLS244 – OCTOBER 1995

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f <sub>max</sub>			C <sub>L</sub> = 15 pF	130	180		110		MHz
			C <sub>L</sub> = 50 pF	85	115		75		
t <sub>PLH</sub>	CLK	Q	C <sub>L</sub> = 15 pF		5.6	8.6	1	10	ns
t <sub>PHL</sub>					5.6	8.6	1	10	
t <sub>PZH</sub>	OE	Q			5.9	9	1	10.5	ns
t <sub>PZL</sub>					5.9	9	1	10.5	
t <sub>PHZ</sub>	OE	Q							ns
t <sub>PLZ</sub>									
t <sub>PLH</sub>	CLK	Q	C <sub>L</sub> = 50 pF		7.1	10.6	1	12	ns
t <sub>PHL</sub>					7.1	10.6	1	12	
t <sub>PZH</sub>	OE	Q			7.4	11	1	12.5	ns
t <sub>PZL</sub>					7.4	11	1	12.5	
t <sub>PHZ</sub>	OE	Q			7.1	10.1	1	11.5	ns
t <sub>PLZ</sub>					7.1	10.1	1	11.5	

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER	$V_{CC}$	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_{\text{sk(o)}}$ Output skew	$3.3\text{ V} \pm 0.3\text{ V}$		1.5		1.5	ns
	$5\text{ V} \pm 0.5\text{ V}$		1		1	

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

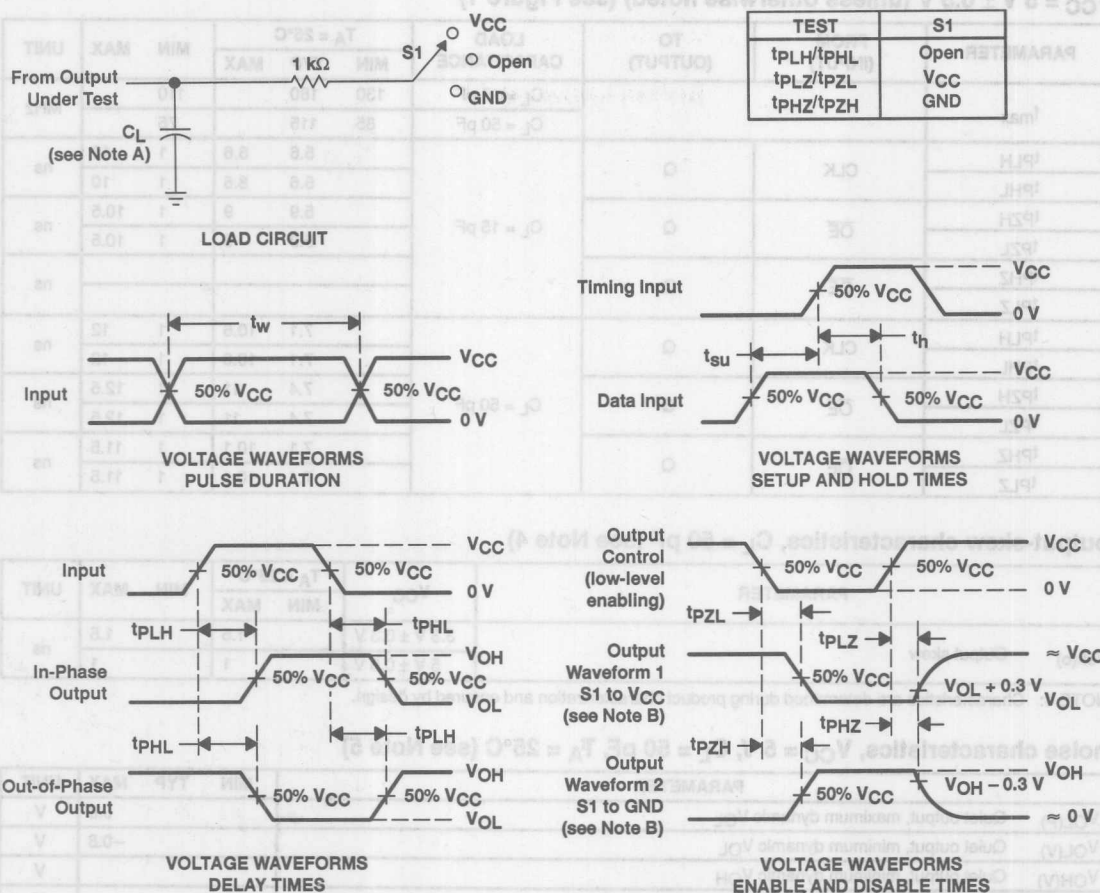
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$		28		pF

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# PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.
  - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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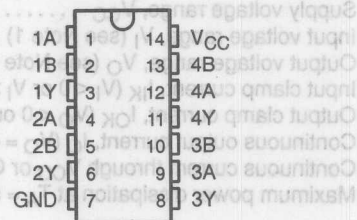
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SN74AHCT541	Octal Buffer/Driver With 3-State Outputs .....	3-89
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SN74AHCT574	Octal Edge-Triggered D-Type Flip-Flop With 3-State Outputs .....	3-99

# SN74AHCT00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS229 – OCTOBER 1995

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIP

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

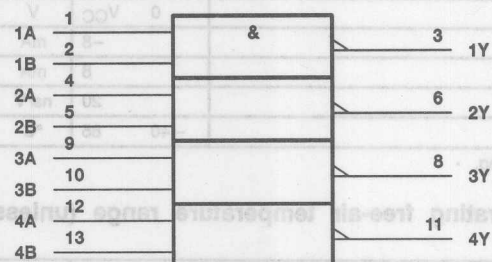
The SN74AHCT00 performs the Boolean functions  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

The SN74AHCT00 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

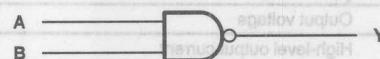
FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PARAMETER		TEST CONDITIONS	
VOH	V	4.5 V	IOH = -80 $\mu\text{A}$
			IOH = -8 mA
			IOH = 80 $\mu\text{A}$
VOL	V	4.5 V	IOH = 80 $\mu\text{A}$
			IOH = 8 mA
			IOH = -80 $\mu\text{A}$
f	Hz	8.5 V	V <sub>I</sub> = VCC or GND
			V <sub>I</sub> = VCC or GND, IO = 0
			One input at 3.4 V, Other inputs at VCC or GND
ΔICC <sup>2</sup>	mA	8.5 V	One input at 3.4 V, Other inputs at VCC or GND
			VO = 8.5 V
			VI = VCC or GND
t <sub>PL</sub>	ns	8.5 V	VO = 8.5 V
			VI = VCC or GND
			VI = VCC or GND

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# SN74AHCT00

## QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS229 - OCTOBER 1995

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	-20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	$\pm 50$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W

Storage temperature range,  $T_{stg}$  -65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-8	mA
$I_{OL}$	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8 \text{ mA}$		2.5			2.4		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1	V
	$I_{OL} = 8 \text{ mA}$				0.36		0.44	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	$\mu\text{A}$
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			1.35		1.5	mA
$I_{off}$	$V_O = 5.5 \text{ V}$	0 V			0.5		5	$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF

<sup>‡</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

# SN74AHCT00

## QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS229 – OCTOBER 1995

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$		5	6.9	1	8	ns
$t_{PHL}$					5	6.9	1	8	
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$		5.5	7.9	1	9	ns
$t_{PHL}$					5.5	7.9	1	9	

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

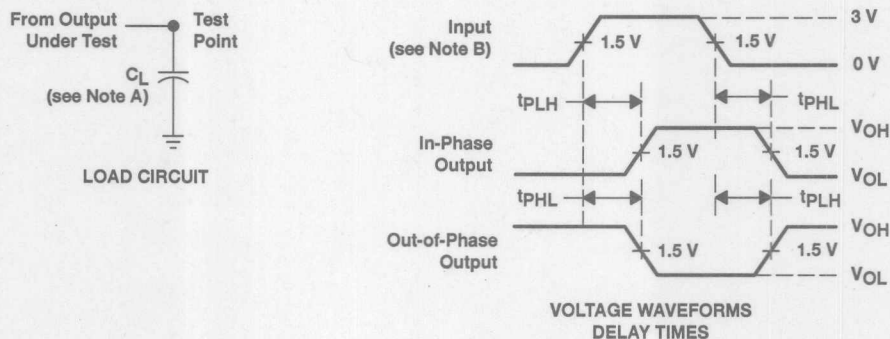
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.4	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.5		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ ,	$f = 1\text{ MHz}$	10.5	pF

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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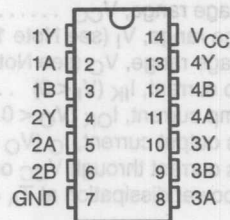


# SN74AHCT02 QUADRUPL 2-INPUT POSITIVE-NOR GATE

SCLS262A – DECEMBER 1995 – REVISED FEBRUARY 1996

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

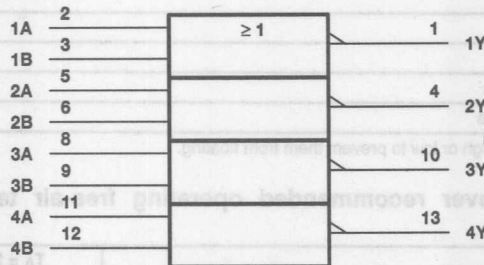
This device contains four independent 2-input NOR gates that perform the Boolean functions  $Y = \overline{A} \cdot \overline{B}$  or  $Y = A + B$  in positive logic.

The SN74AHCT02 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each gate)

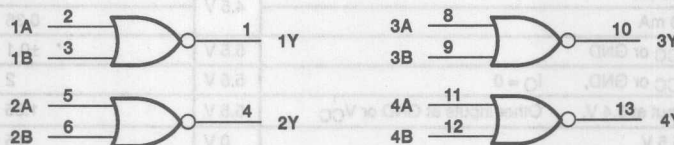
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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# SN74AHCT02

## QUADRUPLE 2-INPUT POSITIVE-NOR GATE

SCLS262A – DECEMBER 1995 – REVISED FEBRUARY 1996

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	–20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W

Storage temperature range,  $T_{stg}$  –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

### recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		V
$V_{IL}$ Low-level input voltage		0.8	V
$V_I$ Input voltage	0	$V_{CC}$	V
$V_O$ Output voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current		–8	mA
$I_{OL}$ Low-level output current		8	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		20	ns/V
$T_A$ Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8 \text{ mA}$		2.5			2.4		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1	V
	$I_{OL} = 8 \text{ mA}$				0.36		0.44	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	μA
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at GND or $V_{CC}$	5.5 V			1.35		1.5	mA
$I_{off}$	$V_O = 5.5 \text{ V}$	0 V			0.5		5	μA
$C_i$	$V_I = V_{CC}$ or GND	5 V			4	10	10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

PRODUCT PREVIEW



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# SN74AHCT02 QUADRUPLE 2-INPUT POSITIVE-NOR GATE

SCLS262A – DECEMBER 1995 – REVISED FEBRUARY 1996

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$				1		ns
$t_{PHL}$							1		
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$				1		ns
$t_{PHL}$							1		

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

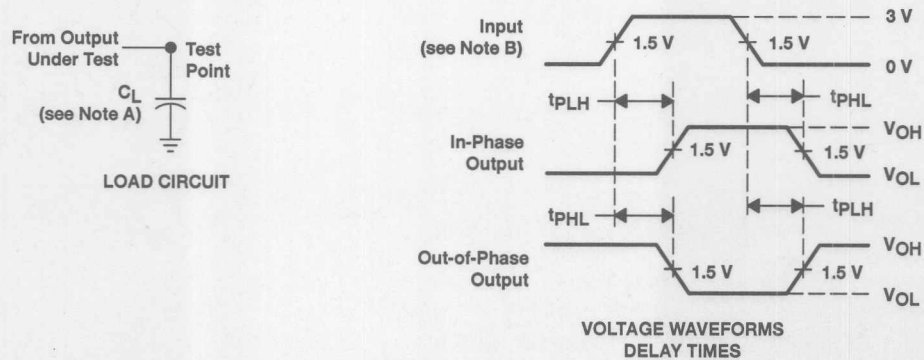
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	17	pF

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# QUADRUPEL 2-INPUT POSITIVE-NOR GATE

80LS252A - DECEMBER 1992 - REVISED FEBRUARY 1993

switching characteristics over recommended operating free-air temperature range.  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TA = 25°C MIN TYP MAX	MIN MAX	UNIT
tPLH	A or B	Y	CL = 15 pF		1	ns
					1	
tPLH	A or B	Y	CL = 50 pF		1	ns
					1	

noise characteristics,  $V_{CC} = 5 \text{ V}$ ,  $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

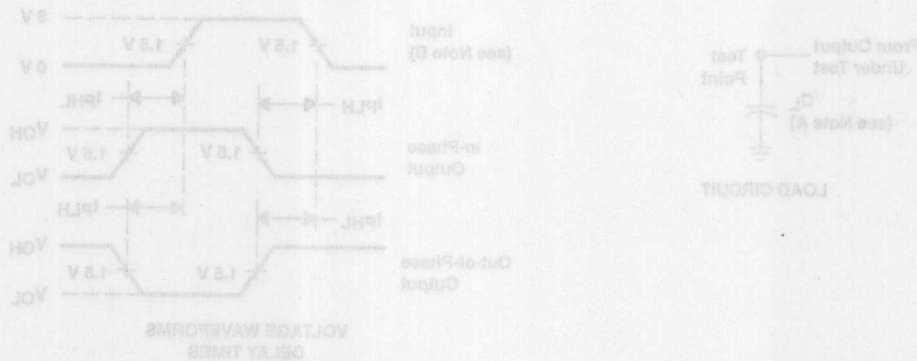
PARAMETER	MIN	TYP	MAX	UNIT
VOLP			0.8	V
VOLM			-0.8	V
VOLH				V
VOLM				V
VHDI		2		V
VLLI			0.8	V

NOTE 4: Characteristics are determined during product characterization and are not by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd	$C_L = 50 \text{ pF}$ , $f = 1 \text{ MHz}$	12	pF

## PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.  
 B. Input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $Z_0 = 50 \Omega$ ,  $r = 2 \text{ ns}$ ,  $V = 3 \text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

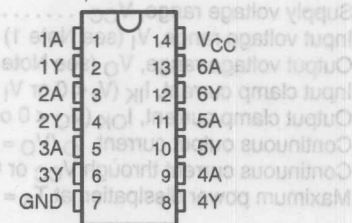
Figure 1. Load Circuit and Voltage Waveforms

# SN74AHCT04 HEX INVERTER

SCLS232A – OCTOBER 1995 – REVISED FEBRUARY 1996

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

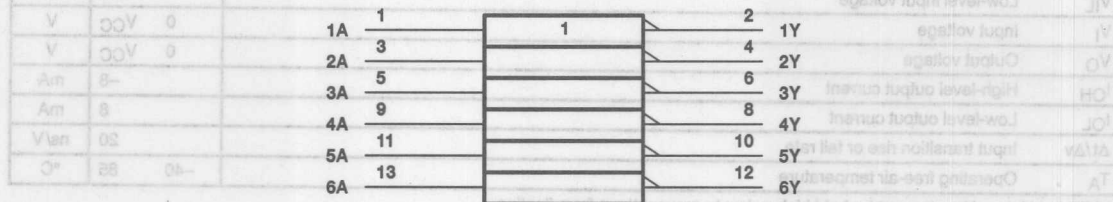
The SN74AHCT04 contains six independent inverters. The device performs the Boolean function  $Y = \bar{A}$ .

The SN74AHCT04 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)

PARAMETER	TEST CONDITIONS	Y	V <sub>CC</sub>	A	UNIT
VOH	IOH = -50 $\mu$ A IOH = -5 mA	H	5.5 V	0.1 V	V
			5.5 V	0.1 V	V
VOL	IOL = 50 $\mu$ A IOL = 5 mA	L	5.5 V	0.1 V	V
			5.5 V	0.1 V	V
II	V <sub>I</sub> = V <sub>CC</sub> or GND		5.5 V	0.1 V	$\mu$ A
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		5.5 V	0.1 V	mA
t <sub>PLH</sub>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	H	5.5 V	0.1 V	ns
			5.5 V	0.1 V	ns

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# SN74AHCT04 HEX INVERTER

SCLS232A – OCTOBER 1995 – REVISED FEBRUARY 1996

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W

Storage temperature range,  $T_{stg}$  ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–8	mA
$I_{OL}$	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8 \text{ mA}$		2.5			2.4		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1	V
	$I_{OL} = 8 \text{ mA}$				0.36		0.44	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	μA
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			1.35		1.5	mA
$C_i$	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .



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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A	Y	$C_L = 15\text{ pF}$	4.7	6.7		1	7.5	ns
$t_{PHL}$				4.7	6.7		1	7.5	
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$	5.5	7.7		1	8.5	ns
$t_{PHL}$				5.5	7.7		1	8.5	

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

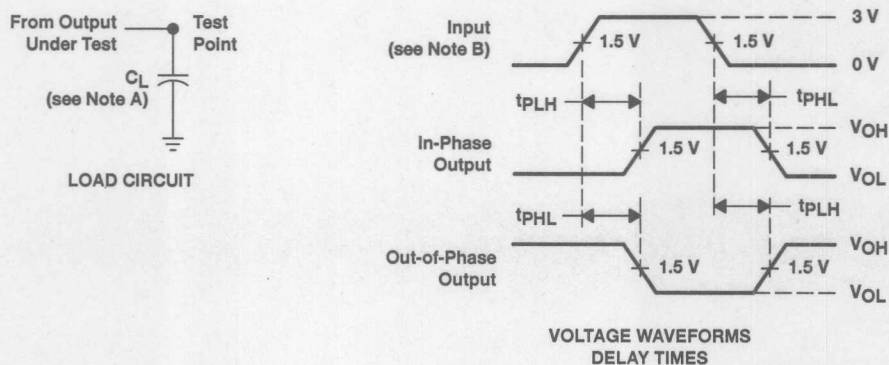
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	14	pF

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



switching characteristics over recommended operating free-air temperature range:  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 7)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			UNIT
				MIN	TYP	MAX	
$t_{PLH}$	A	Y	$C_L = 15 \text{ pF}$	4.7	8.7	1	ns
				4.7	8.7	1	
$t_{PHL}$	A	Y	$C_L = 50 \text{ pF}$	8.8	7.7	1	ns
				8.8	7.7	1	

noise characteristics,  $V_{CC} = 5 \text{ V}$ ,  $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

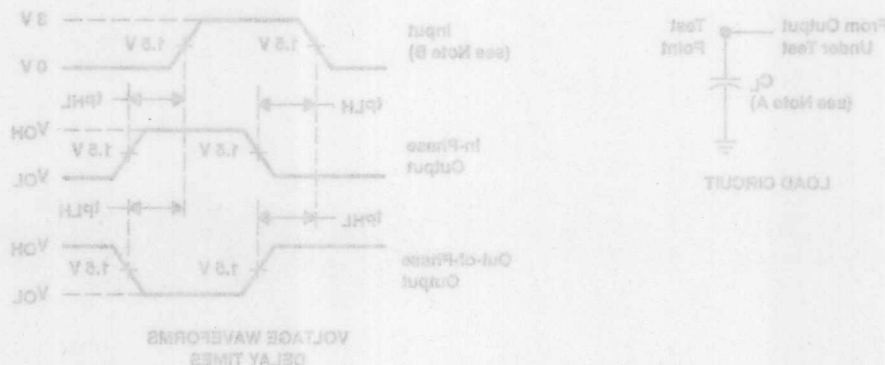
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OLP}$	Quiet output, maximum dynamic $V_{OL}$		0.8		V
$V_{OLN}$	Quiet output, minimum dynamic $V_{OL}$		-0.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8		V

NOTE 4: Characteristics are determined during product characterization and are not for surface-mount packages only.

operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50 \text{ pF}$ , $f = 1 \text{ MHz}$	14	pF

# PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $t_r = 80 \text{ pF}$ ,  $t_f = 3 \text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

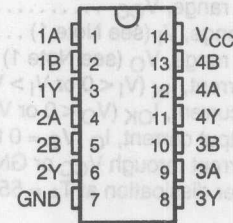
Figure 7. Load Circuit and Voltage Waveforms

# SN74AHCT08 QUADRUPLE 2-INPUT POSITIVE-AND GATE

SCLS237 – OCTOBER 1995

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

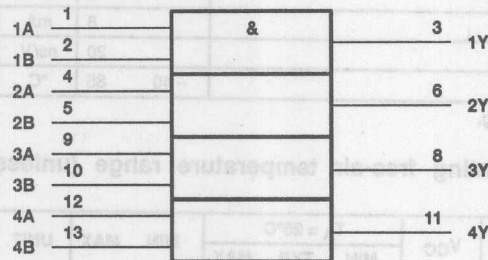
The SN74AHCT08 is a quadruple 2-input positive-AND gate. The device performs the Boolean functions  $Y = A \cdot B$  or  $Y = \overline{A} \cdot \overline{B}$  in positive logic.

The SN74AHCT08 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PARAMETER		TEST CONDITIONS	
V <sub>OH</sub>	A <sub>L</sub> = -50 μA	V <sub>OL</sub> = -50 μA	V <sub>CC</sub> = 5.0 V
V <sub>OL</sub>	A <sub>L</sub> = 50 μA	V <sub>OH</sub> = 5.0 V	V <sub>CC</sub> = 5.0 V
I <sub>CC</sub>	V <sub>CC</sub> = 5.0 V	V <sub>OH</sub> = 5.0 V	V <sub>OL</sub> = 0 V
I <sub>CC</sub>	V <sub>CC</sub> = 5.0 V	V <sub>OH</sub> = 5.0 V	V <sub>OL</sub> = 0 V
I <sub>CC</sub>	V <sub>CC</sub> = 5.0 V	V <sub>OH</sub> = 5.0 V	V <sub>OL</sub> = 0 V
I <sub>CC</sub>	V <sub>CC</sub> = 5.0 V	V <sub>OH</sub> = 5.0 V	V <sub>OL</sub> = 0 V

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PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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# SN74AHCT08

## QUADRUPLE 2-INPUT POSITIVE-AND GATE

SCLS237 – OCTOBER 1995

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	–20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–8	mA
$I_{OL}$	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8 \text{ mA}$		2.5			2.4		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1	0.1		V
	$I_{OL} = 8 \text{ mA}$				0.36	0.44		
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			±0.1	±1		μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2	20		μA
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			1.35	1.5		mA
$I_{off}$	$V_O = 5.5 \text{ V}$	0 V			0.5	5		μA
$C_i$	$V_I = V_{CC}$ or GND	5 V		4	10	10		pF

<sup>‡</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

# SN74AHCT08 QUADRUPLE 2-INPUT POSITIVE-AND GATE

SCLS237 – OCTOBER 1995

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$	5	6.9	1	8	ns	
$t_{PHL}$				5	6.9	1	8		
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$	5.5	7.9	1	9	ns	
$t_{PHL}$				5.5	7.9	1	9		

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

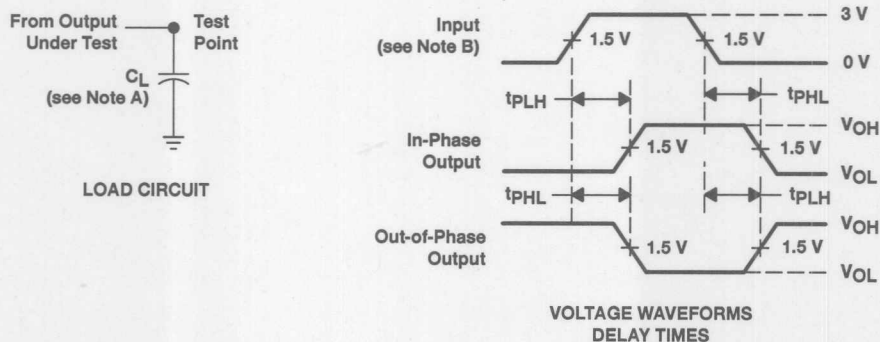
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.4	-0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$		18	pF

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5 \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		UNIT
				MIN	TYP	
$t_{PLH}$	A or B	Y	$C_L = 15 \text{ pF}$	5	8.5	ns
				5	8.5	ns
$t_{PLH}$	A or B	Y	$C_L = 20 \text{ pF}$	5.5	7.5	ns
				5.5	7.5	ns

noise characteristics,  $V_{CC} = 5 \text{ V}$ ,  $C_L = 80 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

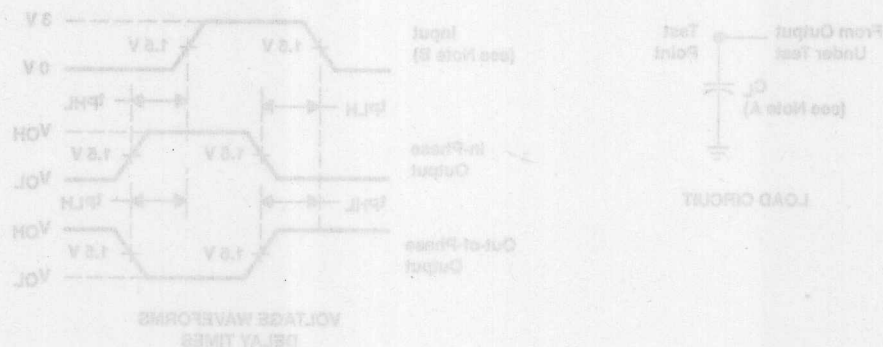
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OLP}$	Quiet output, maximum dynamic $V_{OL}$		0.4	0.8	V
$V_{OLN}$	Quiet output, minimum dynamic $V_{OL}$		-0.4	-0.8	V
$V_{HID}$	High-level dynamic input voltage	2			V
$V_{LID}$	Low-level dynamic input voltage	0.8			V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{od}$	Power dissipation capacitance	$C_L = 80 \text{ pF}$ , $f = 1 \text{ MHz}$	18	pF

# PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $\Delta V = 50 \text{ mV}$ ,  $r_f = 3 \text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

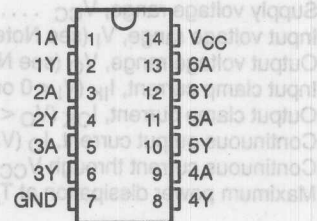


# SN74AHCT14 HEX SCHMITT-TRIGGER INVERTER

SCLS246A – OCTOBER 1995 – REVISED JANUARY 1996

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

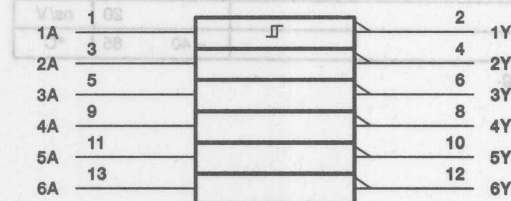
The SN74AHCT14 contains six independent inverters. The device performs the Boolean function  $Y = \bar{A}$ . Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive- ( $V_{T+}$ ) and for negative-going ( $V_{T-}$ ) signals.

The SN74AHCT14 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

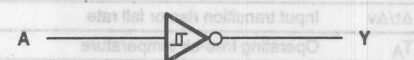
FUNCTION TABLE  
(each inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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SN74AHCT14  
HEX SCHMITT-TRIGGER INVERTER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	–20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2.1		V
$V_{IL}$	Low-level input voltage		0.5	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–8	mA
$I_{OL}$	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

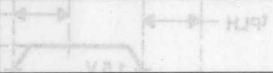
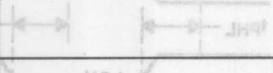
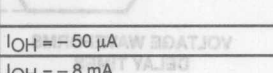


# SN74AHCT14

## HEX SCHMITT-TRIGGER INVERTER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			UNIT
			MIN	TYP	MAX	
V <sub>T+</sub> Positive-going input threshold voltage		4.5 V			2	V
		5.5 V			2	
V <sub>T-</sub> Negative-going input threshold voltage		4.5 V	0.6		0.6	V
		5.5 V	0.6		0.6	
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )		4.5 V	0.4		1.4	V
		5.5 V	0.5		1.6	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	3.15	3.65		V
	I <sub>OH</sub> = -8 mA	4.5 V	2.5			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1	V
	I <sub>OL</sub> = 8 mA	4.5 V			0.36	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		±0.1		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		2		μA
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10	pF

switching characteristics over recommended operating free-air temperature range  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			UNIT
				MIN	TYP	MAX	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF		4	7	ns
t <sub>PHL</sub>					4	7	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF		5.5	8	ns
t <sub>PHL</sub>					5.5	8	

noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 4)

PARAMETER	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub> Quiet output, maximum dynamic V <sub>OL</sub>		0.9		V
V <sub>OL(V)</sub> Quiet output, minimum dynamic V <sub>OL</sub>		-0.7		V
V <sub>OH(V)</sub> Quiet output, minimum dynamic V <sub>OH</sub>		4.3		V
V <sub>IH(D)</sub> High-level dynamic input voltage		2.1		V
V <sub>IL(D)</sub> Low-level dynamic input voltage			0.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design and for surface-mount packages only.

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	C <sub>L</sub> = 50 pF, f = 1 MHz	12	pF

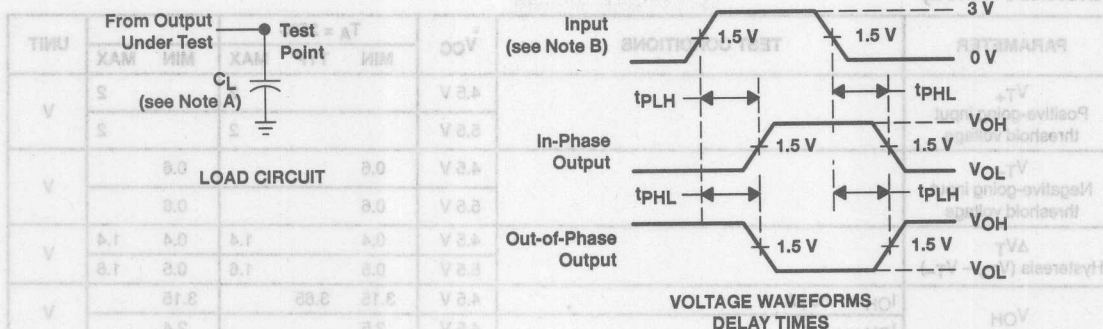


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# SN74AHCT14 HEX SCHMITT-TRIGGER INVERTER

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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

UNIT	MIN	TYP	MAX	PARAMETER
ns	4	7	10	$t_{PLH}$
ns	4	7	10	$t_{PHL}$
ns	4	7	10	$t_{PLH}$
ns	4	7	10	$t_{PHL}$

noise characteristics,  $V_{CC} = 5$  V,  $C_L = 50$  pF,  $T_A = 25^\circ\text{C}$  (see Note 4)

UNIT	MIN	TYP	MAX	PARAMETER
V	0.9			$V_{OLP}$ Output low, maximum dynamic $V_{OL}$
V	0.7			$V_{OLM}$ Output low, minimum dynamic $V_{OL}$
V	4.9			$V_{OHP}$ Output high, maximum dynamic $V_{OH}$
V	5.1			$V_{OHM}$ Output high, minimum dynamic $V_{OH}$
V	0.8			$V_{IH(D)}$ High-level dynamic input voltage
V	0.8			$V_{IL(D)}$ Low-level dynamic input voltage

NOTE 4: Characteristics are determined during product characterization and are not for design and for surface-mount packages only.

operating characteristics,  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$

UNIT	MIN	TYP	MAX	PARAMETER
pF	12			$C_{PD}$ Power dissipation capacitance



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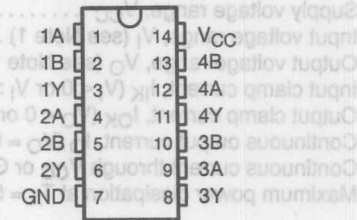


# SN74AHCT32 QUADRUPL 2-INPUT POSITIVE-OR GATE

SCLS248 – OCTOBER 1995

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA
- Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

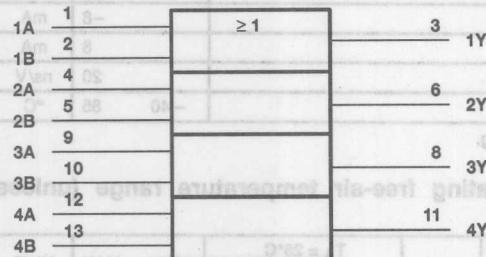
The SN74AHCT32 is a quadruple 2-input positive-OR gate. The device performs the Boolean functions  $Y = \overline{A} \cdot \overline{B}$  or  $Y = A + B$  in positive logic.

The SN74AHCT32 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

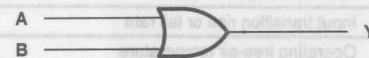
FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PARAMETER		TEST CONDITIONS	
VOH	VOH	VOH = 4.5 V	IOH = -8 mA
			IOH = -8 mA
VOL	VOL	VOL = 0.4 V	IOL = 8 mA
			IOL = 8 mA
II	II	II = 0	VI = VCC or GND
			VI = VCC or GND
IICC	IICC	IICC = 0	Other inputs at VCC or GND
			One input at 2.4 V
VO	VO	VO = 4.5 V	VI = 4.5 V
			VI = VCC or GND
CI	CI	CI = 10	VI = VCC or GND
			VI = VCC or GND

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TEXAS  
INSTRUMENTS

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# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	−0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	−0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	−0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	−20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	−20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, $T_{stg}$	−65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		−8	mA
$I_{OL}$	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
$T_A$	Operating free-air temperature	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8 \text{ mA}$		2.5			2.4		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1	V
	$I_{OL} = 8 \text{ mA}$				0.36		0.44	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	$\mu\text{A}$
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			1.35		1.5	mA
$I_{off}$	$V_O = 5.5 \text{ V}$	0 V			0.5		5	$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	5 V			2	10	10	pF

<sup>‡</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

# SN74AHCT32

## QUADRUPLE 2-INPUT POSITIVE-OR GATE

SCLS248 – OCTOBER 1995

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$	5	6.9		1	8	ns
$t_{PHL}$				5	6.9		1	8	
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$	5.5	7.9		1	9	ns
$t_{PHL}$				5.5	7.9		1	9	

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

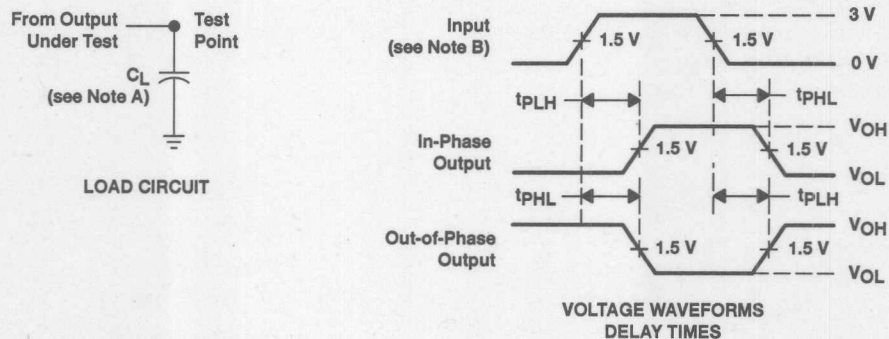
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.4	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	11.5	pF

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# QUADRIPLY 2-INPUT POSITIVE-OR GATE

SCJ2548 - OCTOBER 1988

switching characteristics over recommended operating free-air temperature range  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			UNIT
				MIN	TYP	MAX	
$t_{PLH}$	A or B	Y	$C_L = 15 \text{ pF}$	8	8.5	9	ns
				8	8.5	9	ns
$t_{PHL}$	A or B	Y	$C_L = 50 \text{ pF}$	25	25	26	ns
				25	25	26	ns

noise characteristics,  $V_{CC} = 5 \text{ V}$ ,  $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

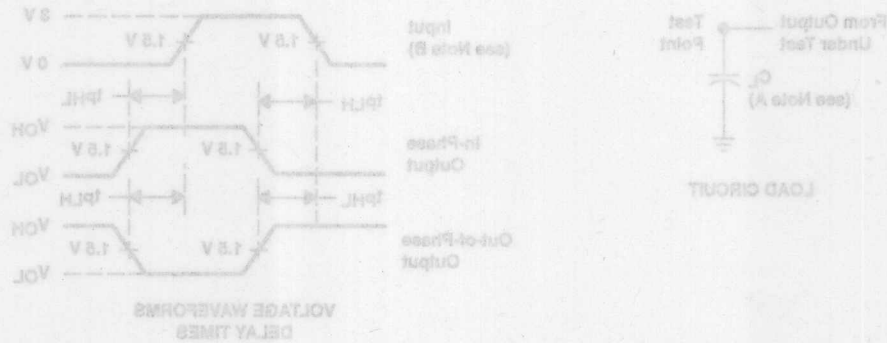
PARAMETER	MIN	TYP	MAX	UNIT
$V_{OLP}$ Quiet output, maximum dynamic $V_{OL}$		0.4	0.5	V
$V_{OLN}$ Quiet output, minimum dynamic $V_{OL}$		-0.4	-0.5	V
$V_{OHM}$ Quiet output, minimum dynamic $V_{OH}$		4.1		V
$V_{IH(D)}$ High-level dynamic input voltage	2			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50 \text{ pF}$ , $f = 1 \text{ MHz}$	11.5	pF

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics: PRR  $\geq 1 \text{ MHz}$ ,  $\tau_{SO} = 50 \text{ pF}$ ,  $\tau_{RI} = 3 \text{ ns}$ ,  $\tau_{FI} = 3 \text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

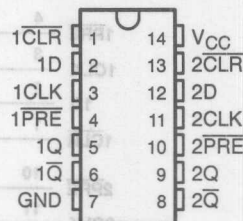
Figure 1. Load Circuit and Voltage Waveforms

# SN74AHCT74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCLS263 – DECEMBER 1995

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

The SN74AHCT74 is a dual positive-edge-triggered D-type flip-flop.

A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) inputs sets or resets the outputs regardless of the levels of the other inputs. When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN74AHCT74 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	$Q_0$	$\overline{Q}_0$

† This configuration is nonstable; that is, it does not persist when  $\overline{PRE}$  or  $\overline{CLR}$  returns to its inactive (high) level.

PRODUCT PREVIEW

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PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



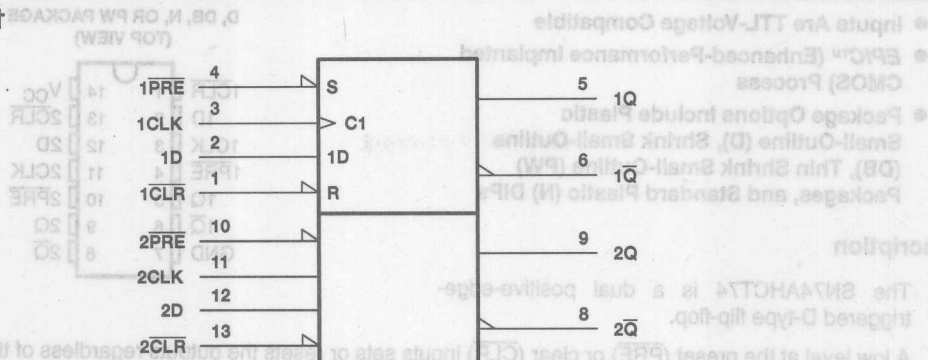
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# **SN74AHCT74** **DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP** **WITH CLEAR AND PRESET**

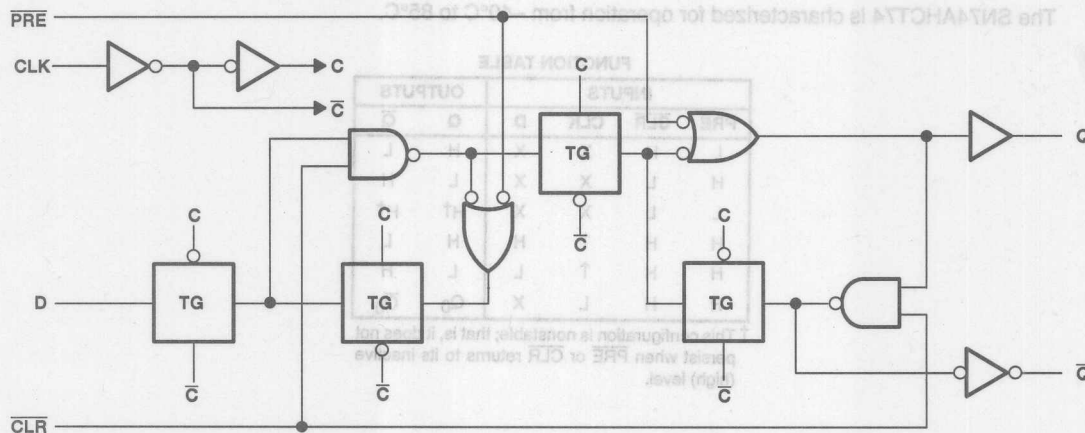
SCLS263 - DECEMBER 1995

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



PRODUCT PREVIEW



# SN74AHCT74

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCLS263 – DECEMBER 1995

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	–20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W

Storage temperature range,  $T_{stg}$  ..... –65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–8	mA
$I_{OL}$	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8 \text{ mA}$		2.5			2.4		V
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1	V
	$I_{OL} = 8 \text{ mA}$				0.36		0.44	V
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	μA
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at GND or $V_{CC}$	5.5 V			1.35		1.5	mA
$I_{off}$	$V_O = 5.5 \text{ V}$	0 V			0.5		5	μA
$C_i$	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF

<sup>‡</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

PRODUCT PREVIEW



# SN74AHCT74

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCLS263 – DECEMBER 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t <sub>w</sub>	Pulse duration					
	PRE or CLR low	5		5		ns
	CLK	5		5		
t <sub>su</sub>	Setup time before CLK↑					
	Data	5		5		ns
	PRE or CLR inactive	5		5		
t <sub>h</sub>	Hold time, data after CLK↑	0		0		ns
t <sub>rem</sub>	Minimum removal time	3.5		3.5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f <sub>max</sub>			C <sub>L</sub> = 15 pF	100	160		80		MHz
			C <sub>L</sub> = 50 pF	80	140		65		
t <sub>PLH</sub>	PRE or CLR	Q or Q̄	C <sub>L</sub> = 15 pF		7.6	10.4	1	12	ns
t <sub>PHL</sub>					7.6	10.4	1	12	
t <sub>PLH</sub>	CLK	Q or Q̄	C <sub>L</sub> = 15 pF		5.8	7.8	1	9	ns
t <sub>PHL</sub>					5.8	7.8	1	9	
t <sub>PLH</sub>	PRE or CLR	Q or Q̄	C <sub>L</sub> = 50 pF		8.1	11.4	1	13	ns
t <sub>PHL</sub>					8.1	11.4	1	13	
t <sub>PLH</sub>	CLK	Q or Q̄	C <sub>L</sub> = 50 pF		6.3	8.8	1	10	ns
t <sub>PHL</sub>					6.3	8.8	1	10	

noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 4)

PARAMETER	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub> Quiet output, maximum dynamic V <sub>OL</sub>			0.8	V
V <sub>OL(V)</sub> Quiet output, minimum dynamic V <sub>OL</sub>			-0.8	V
V <sub>OH(V)</sub> Quiet output, minimum dynamic V <sub>OH</sub>			V	V
V <sub>IH(D)</sub> High-level dynamic input voltage	2			V
V <sub>IL(D)</sub> Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	C <sub>L</sub> = 50 pF, f = 1 MHz	24	pF

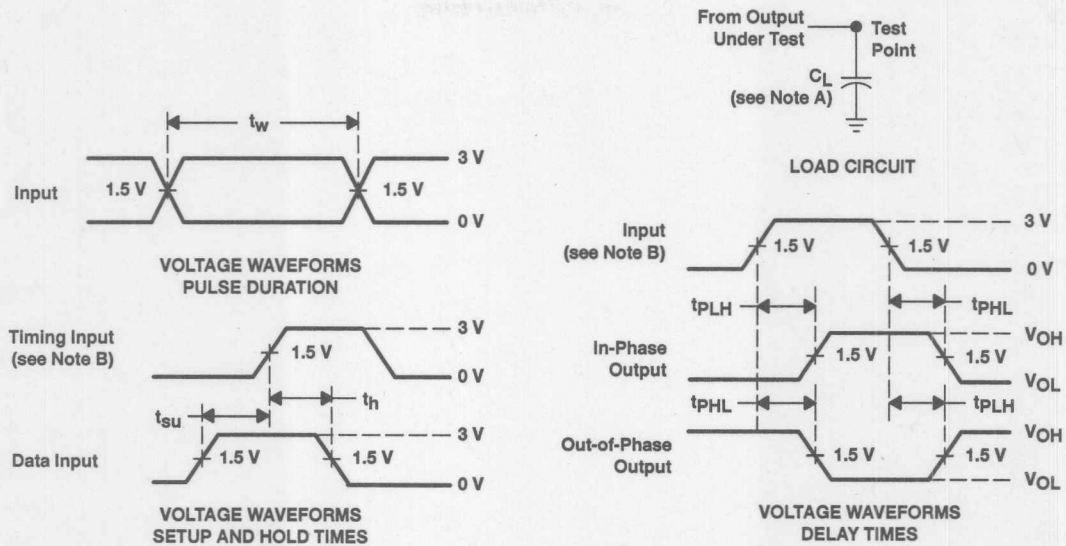


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# SN74AHCT74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCLS263 – DECEMBER 1995

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
C. The outputs are measured one at a time with one input transition per measurement.

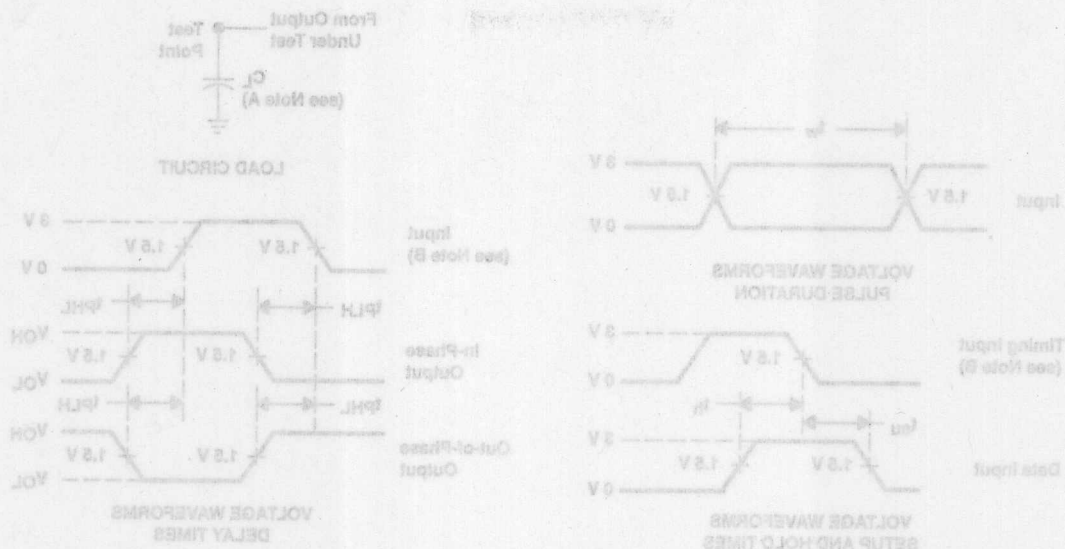
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW



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# PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_0 = 50 \Omega$ ,  $V_L = 3$  ns,  $V_H = 3$  ns.  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 7. Load Circuit and Voltage Waveforms

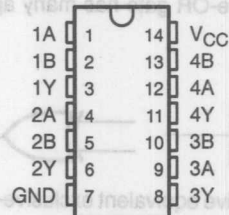
PRODUCT PREVIEW

# SN74AHCT86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCLS250A – OCTOBER 1995 – REVISED FEBRUARY 1996

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

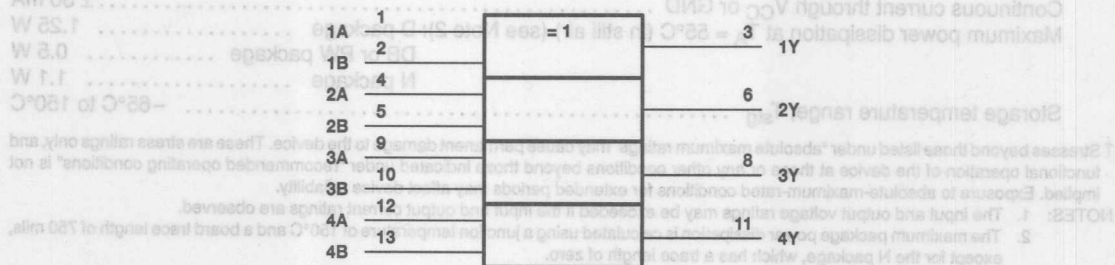
The SN74AHCT86 is a quadruple 2-input exclusive-OR gate. The device performs the Boolean functions  $Y = A \oplus B$  or  $Y = \overline{A}B + A\overline{B}$  in positive logic.

The SN74AHCT86 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



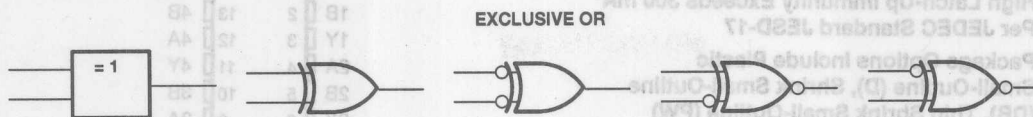
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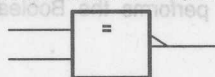
## exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an SN74AHCT86 gate in positive logic; negation may be shown at any two ports.

## LOGIC-IDENTITY ELEMENT



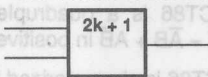
The output is active (low) if all inputs stand at the same logic level (i.e.,  $A = B$ ).

## EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

## ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	-20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package .....	1.25 W
DB or PW package .....	0.5 W
N package .....	1.1 W
Storage temperature range, $T_{stg}$ .....	$-65^\circ\text{C}$ to $150^\circ\text{C}$

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

# SN74AHCT86

## QUADRUPL 2-INPUT EXCLUSIVE-OR GATE

SCLS250A – OCTOBER 1995 – REVISED FEBRUARY 1996

### recommended operating conditions (see Note 3)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		–8	mA
I <sub>OL</sub>	Low-level output current		8	mA
Δt/Δv	Input transition rise or fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	4.5 V	3.15	3.65		3.15		V
	I <sub>OH</sub> = –8 mA		2.5			2.4		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 8 mA				0.36		0.44	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20	μA
ΔI <sub>CC</sub> †	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
I <sub>off</sub>	V <sub>O</sub> = 5.5 V	0 V			0.5		5	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10		10	pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

### switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	5	6.9		1	8	ns
t <sub>PHL</sub>				5	6.9		1	8	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF	5.5	7.9		1	9	ns
t <sub>PHL</sub>				5.5	7.9		1	9	

### noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 4)

PARAMETER	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub> Quiet output, maximum dynamic V <sub>OL</sub>		0.4	0.8	V
V <sub>OL(V)</sub> Quiet output, minimum dynamic V <sub>OL</sub>		–0.4	–0.8	V
V <sub>IH(D)</sub> High-level dynamic input voltage	2			V
V <sub>IL(D)</sub> Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.



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# SN74AHCT86

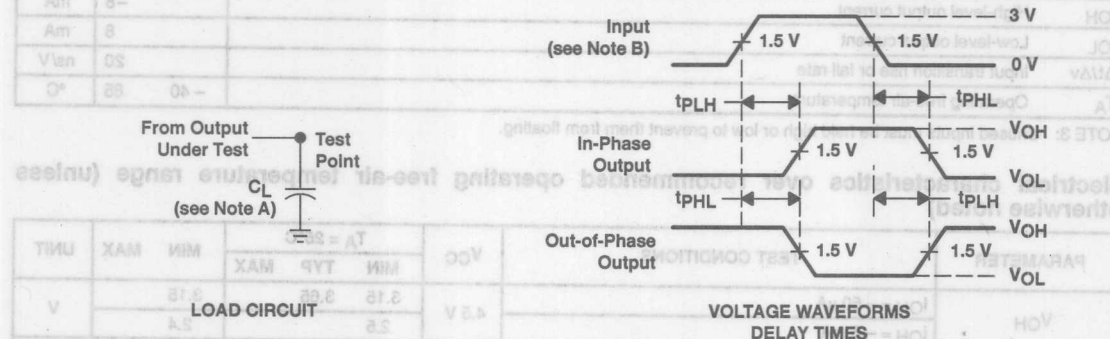
## QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCLS250A - OCTOBER 1995 - REVISED FEBRUARY 1996

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	18	pF

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CAPACITANCE	$T_A = 25^\circ\text{C}$	
				MIN	TYP
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$	8.8	8
$t_{PHL}$	A or B	Y	$C_L = 15\text{ pF}$	8.8	8
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$	8.8	8
$t_{PHL}$	A or B	Y	$C_L = 50\text{ pF}$	8.8	8

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER	MIN	TYP	MAX	UNIT
Quiet output, maximum dynamic $V_{OL}$		0.4	0.8	V
Quiet output, minimum dynamic $V_{OL}$		-0.4	-0.8	V
High-level dynamic input voltage		2		V
Low-level dynamic input voltage		0.8		V

NOTE 4: Characteristics are determined during product characterization and covered by design for surface-mount packages only.



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# SN74AHCT125

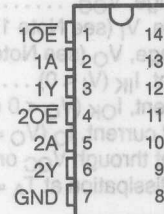
## QUADRUPLE BUS BUFFER GATE

### WITH 3-STATE OUTPUTS

SCLS264 - DECEMBER 1995

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



#### description

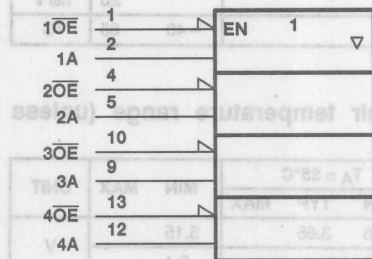
The SN74AHCT125 quadruple bus buffer gate features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high. When  $\overline{OE}$  is low, the respective gate passes the data from the A input to its Y output.

The SN74AHCT125 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each buffer)

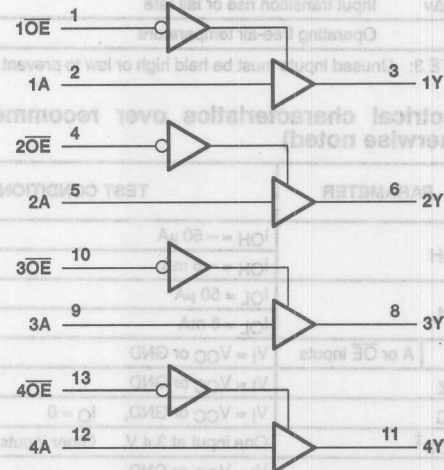
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



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**TEXAS**  
**INSTRUMENTS**

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PRODUCT PREVIEW



# SN74AHCT125

## QUADRUPLE BUS BUFFER GATE

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	−0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	−0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	−0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	−20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	−20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, $T_{stg}$	−65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

#### recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		V
$V_{IL}$ Low-level input voltage		0.8	V
$V_I$ Input voltage	0	$V_{CC}$	V
$V_O$ Output voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current		−8	mA
$I_{OL}$ Low-level output current		8	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		20	ns/V
$T_A$ Operating free-air temperature	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8 \text{ mA}$		2.5			2.4		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1	V
	$I_{OL} = 8 \text{ mA}$				0.36		0.44	
$I_I$ A or $\overline{OE}$ inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
$I_{OZ}$	$V_I = V_{CC}$ or GND	5.5 V			±0.25		±2.5	μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	μA
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			1.35		1.5	mA
$C_i$	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF
$C_o$	$V_O = V_{CC}$ or GND	5 V		15				pF

<sup>‡</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

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**SN74AHCT125**  
**QUADRUPLE BUS BUFFER GATE**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF						ns
t <sub>PHL</sub>									
t <sub>PZH</sub>	OE	Y							ns
t <sub>PZL</sub>									
t <sub>PHZ</sub>	OE	Y							ns
t <sub>PLZ</sub>									
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF						ns
t <sub>PHL</sub>									
t <sub>PZH</sub>	OE	Y							ns
t <sub>PZL</sub>									
t <sub>PHZ</sub>	OE	Y							ns
t <sub>PLZ</sub>									

output-skew characteristics, C<sub>L</sub> = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>sk(o)</sub>	A	Y	5 V ± 0.5 V			1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>			0.8	V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>			-0.8	V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>				V
V <sub>IH(D)</sub>	High-level dynamic input voltage	2			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C <sub>pd</sub>	Power dissipation capacitance	C <sub>L</sub> = 50 pF,	f = 1 MHz				pF

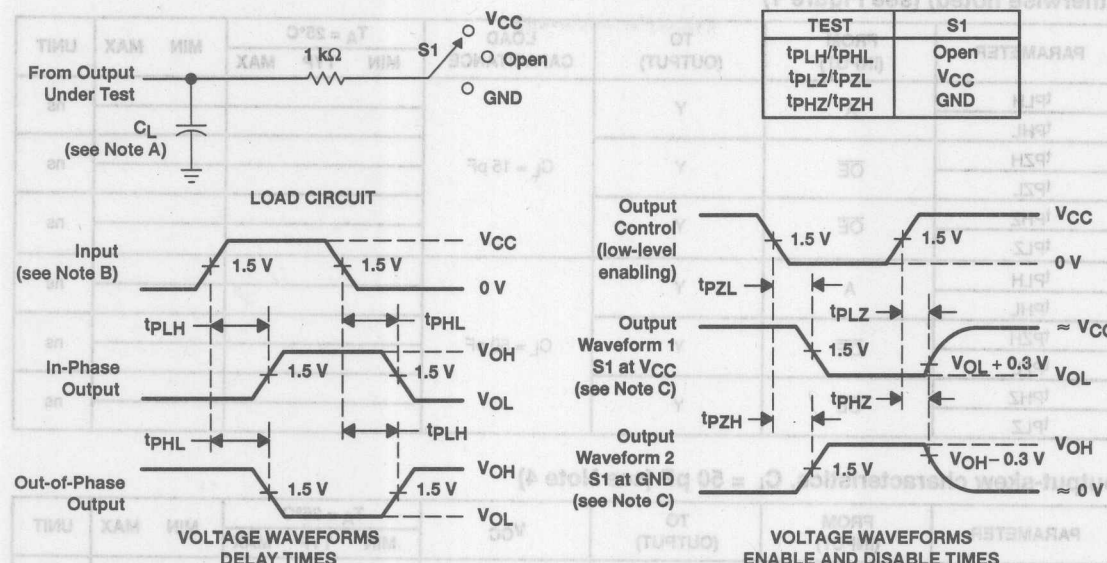
PRODUCT PREVIEW



# SN74AHCT125 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, ZO = 50 Ω, tr = 3 ns, tf = 3 ns.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cpd	Power dissipation capacitance				pf



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# SN74AHCT126 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS SCLS265 – DECEMBER 1995

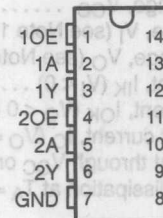
- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

## description

The SN74AHCT126 quadruple bus buffer gate features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low. When OE is high, the respective gate passes the data from the A input to its Y output.

The SN74AHCT126 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

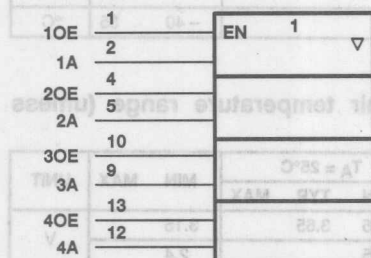
D, DB, N, OR PW PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each buffer)

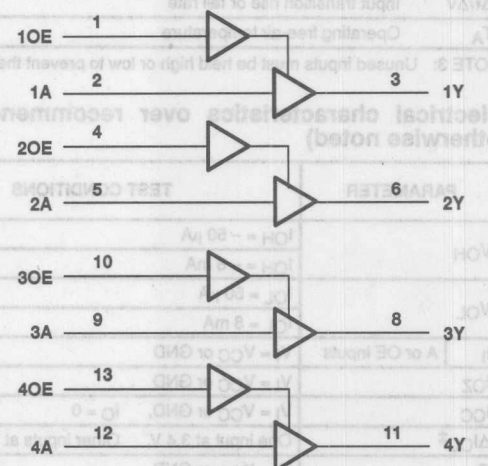
INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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PRODUCT PREVIEW

# SN74AHCT126

## QUADRUPLE BUS BUFFER GATE

### WITH 3-STATE OUTPUTS

SCLS265 - DECEMBER 1995

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	-20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	$\pm 50$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, $T_{stg}$	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-8	mA
$I_{OL}$	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8 \text{ mA}$		2.5			2.4		V
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1	V
	$I_{OL} = 8 \text{ mA}$				0.36		0.44	V
$I_I$	A or OE inputs	5.5 V			$\pm 0.1$		$\pm 1$	$\mu\text{A}$
$I_{OZ}$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.25$		$\pm 2.5$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	$\mu\text{A}$
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			1.35		1.5	mA
$C_i$	$V_I = V_{CC}$ or GND	5 V			4	10	10	pF
$C_o$	$V_O = V_{CC}$ or GND	5 V			15			pF

<sup>‡</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

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**SN74AHCT126**  
**QUADRUPLE BUS BUFFER GATE**  
**WITH 3-STATE OUTPUTS**  
SCLS265 – DECEMBER 1995

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF						ns
t <sub>PHL</sub>									
t <sub>PZH</sub>	OE	Y							ns
t <sub>PZL</sub>									
t <sub>PHZ</sub>	OE	Y							ns
t <sub>PLZ</sub>									
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF						ns
t <sub>PHL</sub>									
t <sub>PZH</sub>	OE	Y							ns
t <sub>PZL</sub>									
t <sub>PHZ</sub>	OE	Y							ns
t <sub>PLZ</sub>									

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{sk(o)}$	A	Y	$5\text{ V} \pm 0.5\text{ V}$			1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$ High-level dynamic input voltage	2			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$				pF

PRODUCT PREVIEW

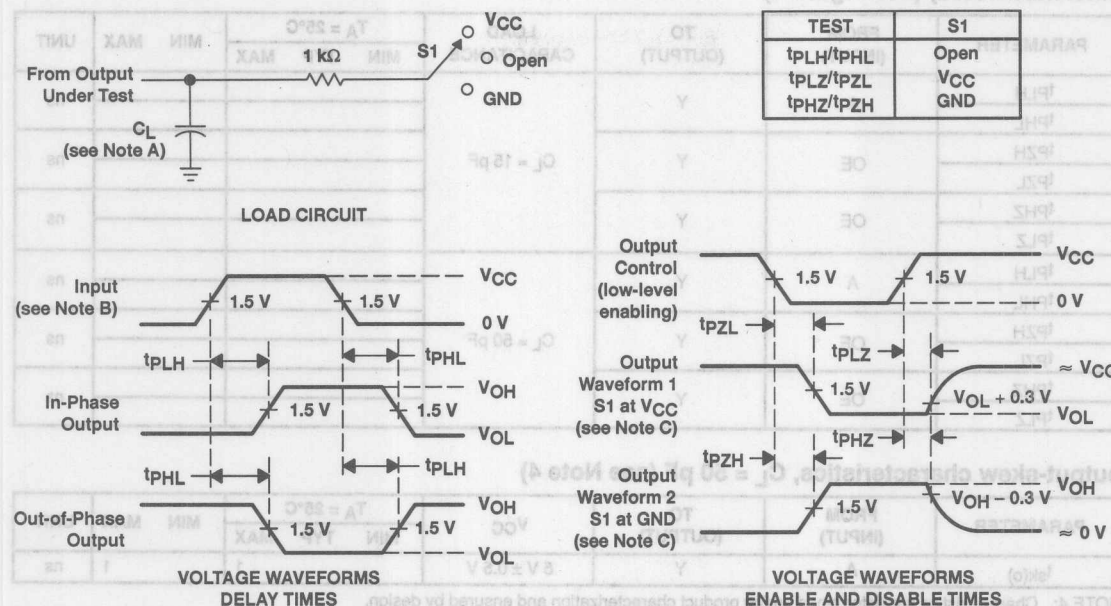




# SN74AHCT126 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCLS265 - DECEMBER 1995

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power dissipation	$C_L = 50$ pF, $f = 1$ MHz				W



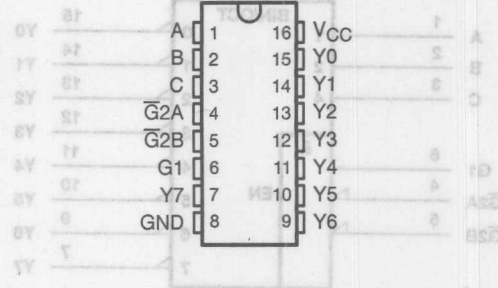
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# SN74AHCT138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

SCLS266 – DECEMBER 1995

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporates Three Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

The SN74AHCT138 3-line to 8-line decoder/demultiplexer is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN74AHCT138 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	L	H	H	H	H
H	L	L	H	L	H	H	H	H	H	L	H	H	H
H	L	L	H	H	L	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	H	H	H	L	H

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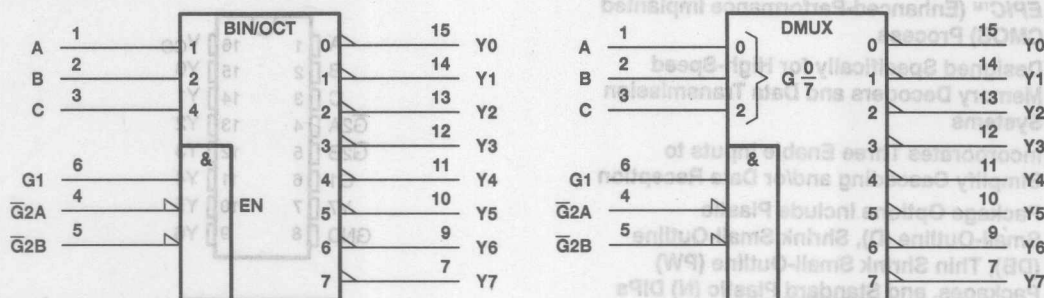
PRODUCT PREVIEW

# SN74AHCT138

## 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

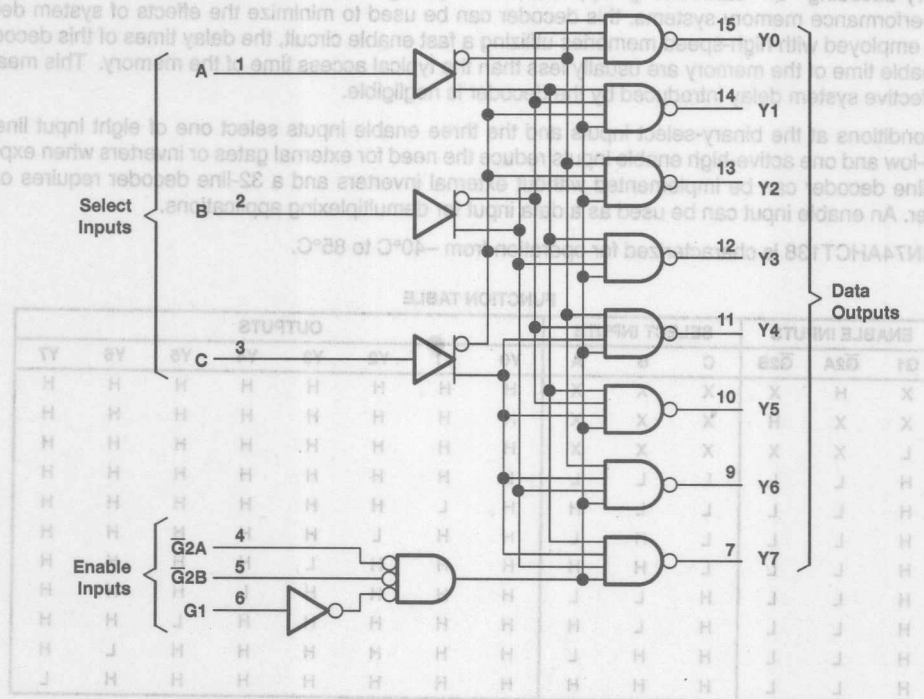
SCLS266 - DECEMBER 1995

### logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



PRODUCT PREVIEW

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# SN74AHCT138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

SCLS266 – DECEMBER 1995

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	–20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.3 W
DB package	0.55 W
N package	1.1 W
PW package	0.5 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–8	mA
$I_{OL}$	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8 \text{ mA}$		2.5			2.4		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1	V
	$I_{OL} = 8 \text{ mA}$				0.36		0.44	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40	μA
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			1.35		1.5	mA
$I_{off}$	$V_O = 5.5 \text{ V}$	0 V			0.5		5	μA
$C_i$	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF

<sup>‡</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

PRODUCT PREVIEW



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### 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

SCLS266 – DECEMBER 1995

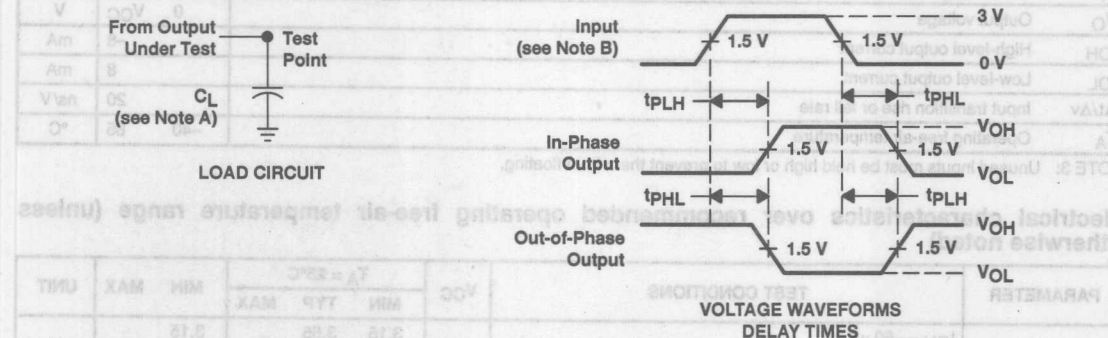
$V_{GG} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A, B, C	Any Y	C <sub>L</sub> = 15 pF	7.6	10.4	1	12	ns	
t <sub>PHL</sub>				7.6	10.4	1	12		
t <sub>PLH</sub>	G1	Any Y	C <sub>L</sub> = 15 pF	6.6	9.1	1	10.5	ns	
t <sub>PHL</sub>				6.6	9.1	1	10.5		
t <sub>PLH</sub>	G <sub>2</sub> A, G <sub>2</sub> B	Any Y	C <sub>L</sub> = 15 pF	7	9.6	1	11	ns	
t <sub>PHL</sub>				7	9.6	1	11		
t <sub>PLH</sub>	A, B, C	Any Y	C <sub>L</sub> = 50 pF	8.1	11.4	1	13	ns	
t <sub>PHL</sub>				8.1	11.4	1	13		
t <sub>PLH</sub>	G1	Any Y	C <sub>L</sub> = 50 pF	7.1	10.1	1	11.5	ns	
t <sub>PHL</sub>				7.1	10.1	1	11.5		
t <sub>PLH</sub>	G <sub>2</sub> A, G <sub>2</sub> B	Any Y	C <sub>L</sub> = 50 pF	7.5	10.6	1	12	ns	
t <sub>PHL</sub>				7.5	10.6	1	12		

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per gate	C <sub>L</sub> = 50 pF, f = 1 MHz	49	pF

### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
C. The outputs are measured one at a time with one input transition per measurement.

### Figure 1. Load Circuit and Voltage Waveforms



# SN74AHCT138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

SCLS266 - DECEMBER 1995

## APPLICATION INFORMATION

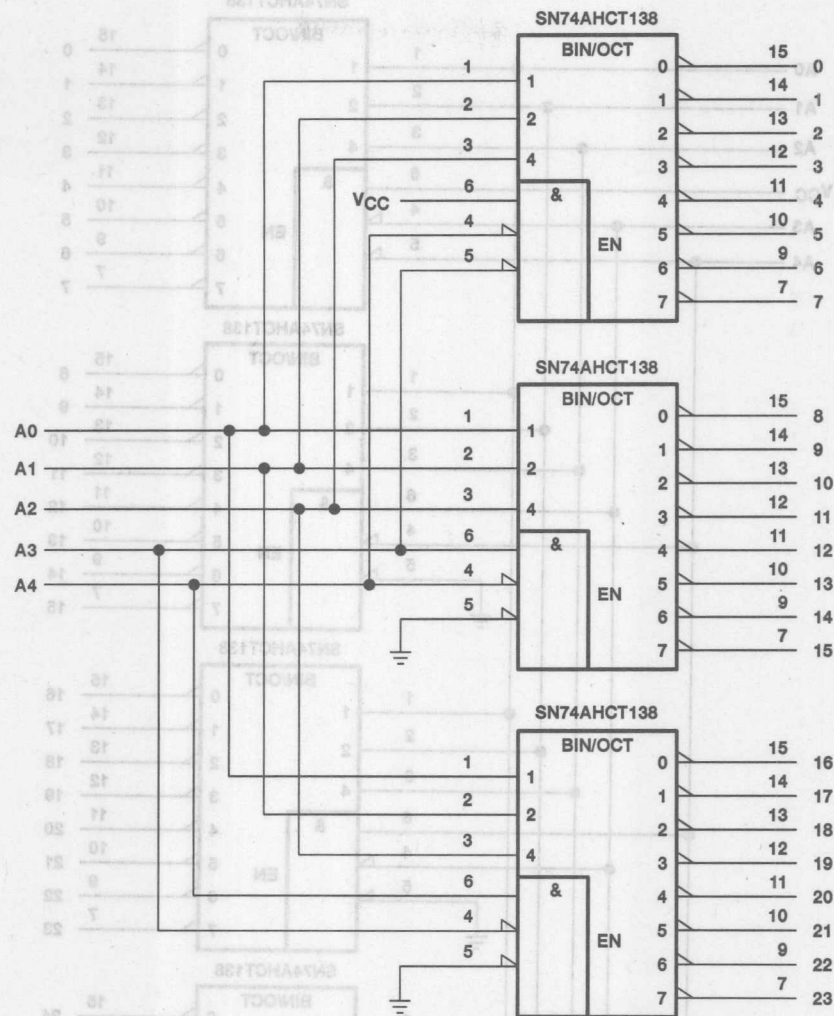


Figure 2. 24-Bit Decoding Scheme

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# SN74AHCT138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

SCLS266 - DECEMBER 1995

## APPLICATION INFORMATION

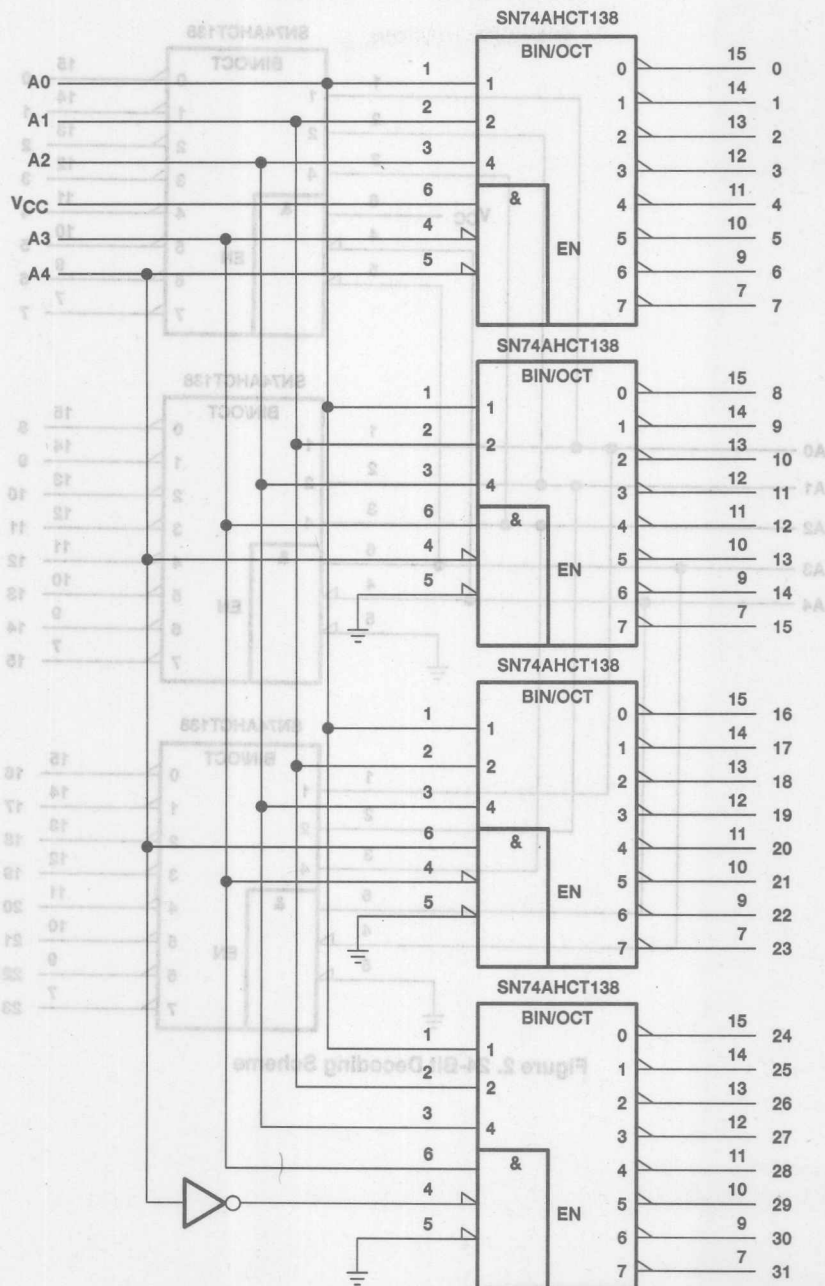


Figure 3. 32-Bit Decoding Scheme



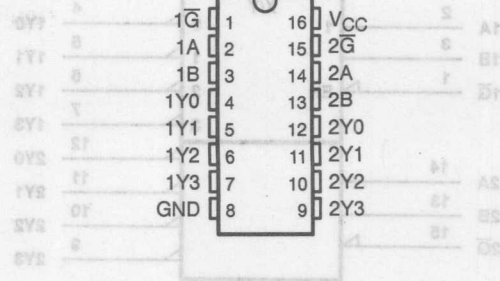
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# SN74AHCT139 DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCLS267A - DECEMBER 1995 - REVISED FEBRUARY 1996

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporates Two Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

D, DB, N, OR PW PACKAGE  
(TOP VIEW)



## description

The SN74AHCT139 is a dual 2-line to 4-line decoder/demultiplexer designed for 2-V to 5.5-V  $V_{CC}$  operation. This device is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The active-low enable ( $\bar{G}$ ) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN74AHCT139 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

G	INPUTS		OUTPUTS			
	SELECT		Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

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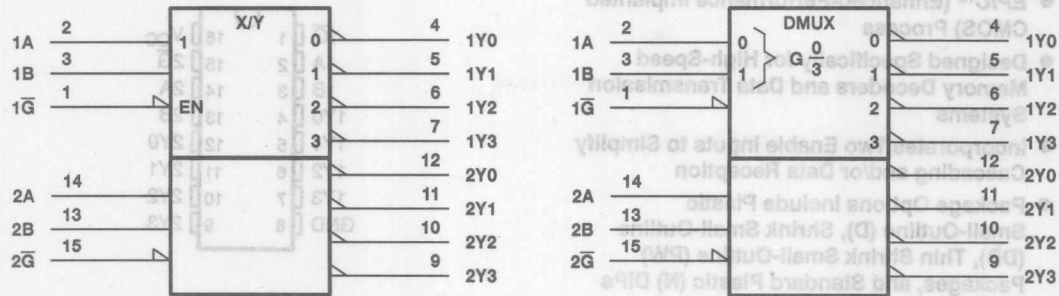
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# SN74AHCT139 DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

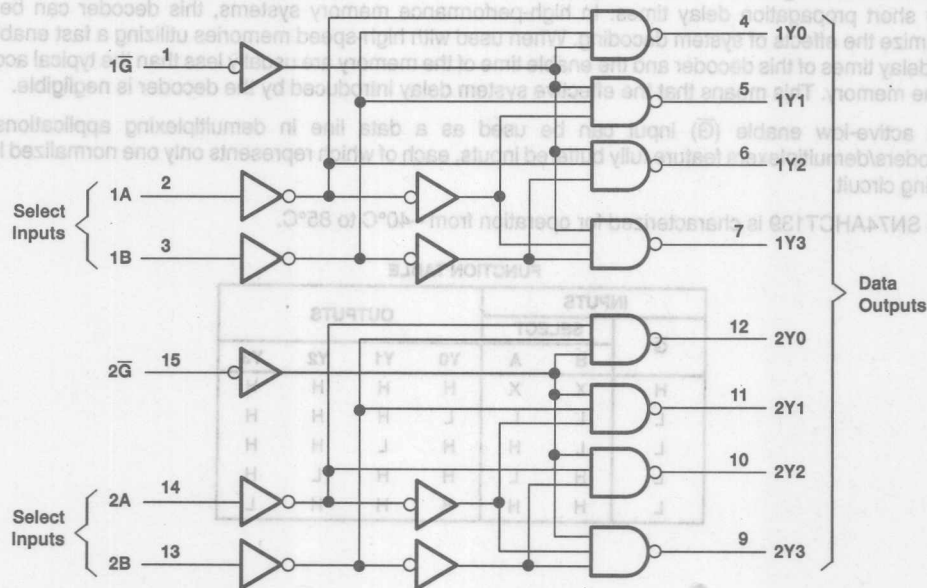
SCLS267A - DECEMBER 1995 - REVISED FEBRUARY 1996

## logic symbols (alternatives)<sup>†</sup>



<sup>†</sup> These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



PRODUCT PREVIEW

**TEXAS  
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# SN74AHCT139 DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCLS267A – DECEMBER 1995 – REVISED FEBRUARY 1996

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	-20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
D package	1.3 W
DB package	0.55 W
N package	1.1 W
PW package	0.5 W
Storage temperature range, $T_{stg}$	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		V
$V_{IL}$ Low-level input voltage		0.8	V
$V_I$ Input voltage	0	$V_{CC}$	V
$V_O$ Output voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current		-8	mA
$I_{OL}$ Low-level output current		8	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		20	ns/V
$T_A$ Operating free-air temperature	-40	85	°C

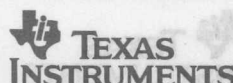
NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8 \text{ mA}$		2.5			2.4		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1	V
	$I_{OL} = 8 \text{ mA}$				0.36		0.44	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	μA
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			1.35		1.5	mA
$C_i$	$V_I = V_{CC}$ or GND	5 V		4.5				pF

<sup>‡</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

PRODUCT PREVIEW



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# SN74AHCT139 DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCLS267A - DECEMBER 1995 - REVISED FEBRUARY 1996

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

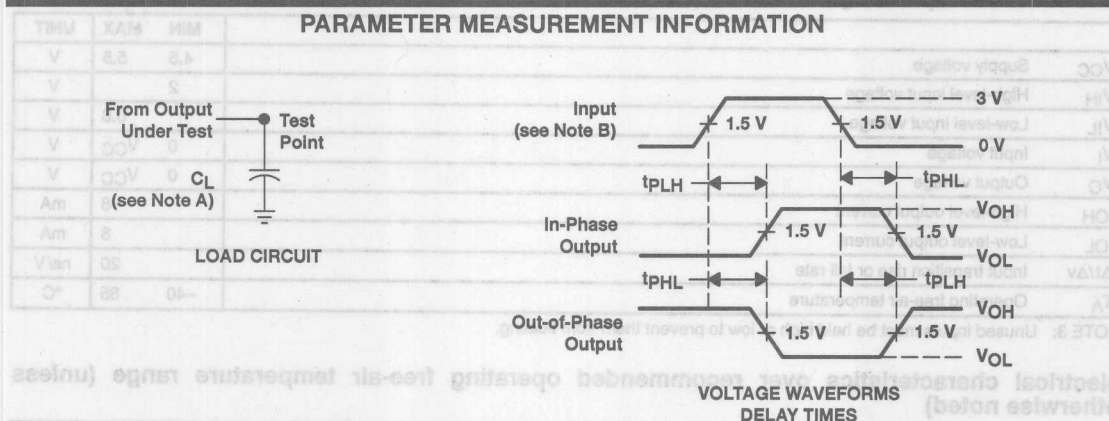
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$				1		ns
$t_{PHL}$							1		
$t_{PLH}$	$\bar{G}$	Y	$C_L = 15\text{ pF}$				1		ns
$t_{PHL}$							1		
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$				1		ns
$t_{PHL}$							1		
$t_{PLH}$	$\bar{G}$	Y	$C_L = 50\text{ pF}$				1		ns
$t_{PHL}$							1		

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	26	pF

PRODUCT PREVIEW

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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# SN74AHCT240

## OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCLS252 – OCTOBER 1995

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

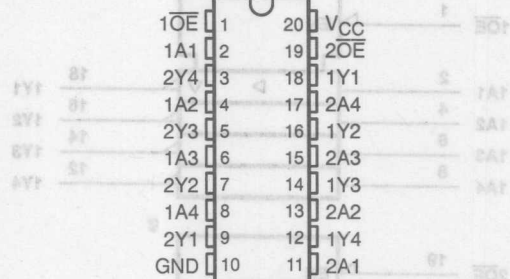
### description

This octal buffer/driver is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74AHCT240 is organized as two 4-bit buffers/line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The SN74AHCT240 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range,  $V_{CC}$  .....  $-0.5\text{ V to }7\text{ V}$

Input voltage range,  $V_I$  (see Note 1) .....  $-0.5\text{ V to }7\text{ V}$

Output voltage range,  $V_O$  (see Note 1) .....  $-0.5\text{ V to }7\text{ V}$

Input clamp current,  $I_{IK}$  ( $V_I < 0$  or  $V_I > V_{CC}$ ) .....  $-20\text{ mA}$

Output clamp current,  $I_{OK}$  ( $V_O < 0$  or  $V_O > V_{CC}$ ) .....  $-20\text{ mA}$

Continuous output current,  $I_O$  ( $V_O = 0$  to  $V_{CC}$ ) .....  $\pm 25\text{ mA}$

Continuous current through  $V_{CC}$  or GND .....  $\pm 75\text{ mA}$

Maximum power dissipation at  $T_A = 85^{\circ}\text{C}$  (in still air) (see Note 2) .....  $0.8\text{ W}$

Storage temperature range,  $T_{stg}$  .....  $-65^{\circ}\text{C to }150^{\circ}\text{C}$

Notes:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum power dissipation is calculated using a junction temperature of  $150^{\circ}\text{C}$  and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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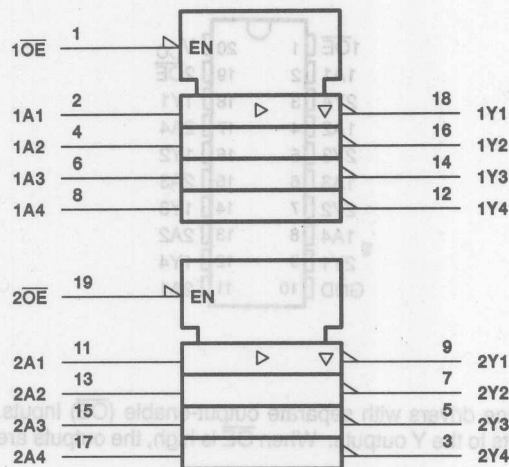
# SN74AHCT240

## OCTAL BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

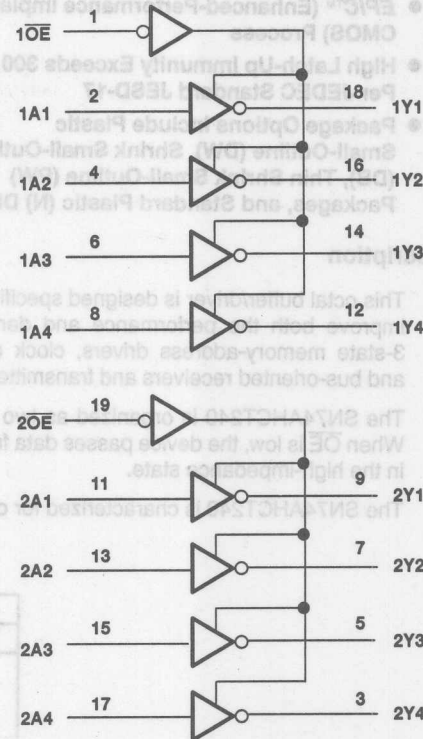
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#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	-20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	$\pm 75$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	-65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.



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**SN74AHCT240**  
**OCTAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**  
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**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-8	mA
$I_{OL}$	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8\ \text{mA}$		2.5			2.4		
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	4.5 V		.001	0.1		0.1	V
	$I_{OL} = 8\ \text{mA}$				0.36		0.44	
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.5 V		$\pm 0.25$		$\pm 2.5$		$\mu\text{A}$
$I_I$	$V_I = V_{CC}$ or GND	5.5 V		$\pm 0.1$		$\pm 1$		$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4	40		$\mu\text{A}$
$\Delta I_{CC}^\dagger$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			1.35	1.5		mA
$I_{off}$	$V_O = 5.5\ \text{V}$	0 V			0.5	5		$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	5 V		2.5	10	10		pF
$C_o$	$V_O = V_{CC}$ or GND	5 V		3				pF

$^\dagger$  This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

PARAMETER	TEST CONDITIONS	TYP	UNIT
Power dissipation	$C_L = 50\ \text{pF}$ , $f = 1\ \text{MHz}$	10	mW



**SN74AHCT240**  
**OCTAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**  
 SCLS252 – OCTOBER 1995

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	5.4	7.4	1	8.5	ns	
t <sub>PHL</sub>				5.4	7.4	1	8.5		
t <sub>PZH</sub>	OE	Y		7.7	10.4	1	12	ns	
t <sub>PZL</sub>				7.7	10.4	1	12		
t <sub>PHZ</sub>	OE	Y		8.3	10.4	1	12	ns	
t <sub>PLZ</sub>				8.3	10.4	1	12		
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	5.9	8.4	1	9.5	ns	
t <sub>PHL</sub>				5.9	8.4	1	9.5		
t <sub>PZH</sub>	OE	Y		8.2	11.4	1	13	ns	
t <sub>PZL</sub>				8.2	11.4	1	13		
t <sub>PHZ</sub>	OE	Y		8.8	11.4	1	13	ns	
t <sub>PLZ</sub>				8.8	11.4	1	13		

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER	$V_{CC}$	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_{sk(o)}$ Output skew	$5\text{ V} \pm 0.5\text{ V}$	1	1	1	1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$		0.6		V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$		-0.6		V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		4.1		V
$V_{IH(D)}$ High-level dynamic input voltage	2			V
$V_{IL(D)}$ Low-level dynamic input voltage		0.8		V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

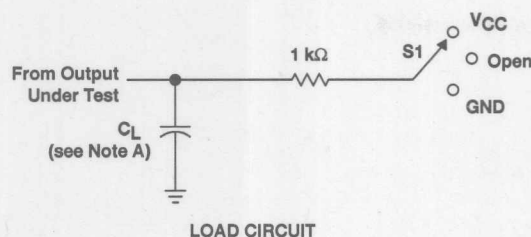
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	10	pF



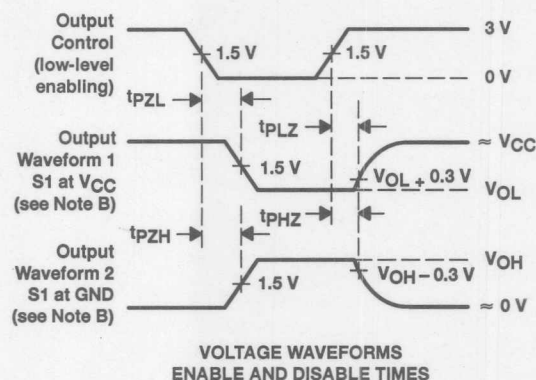
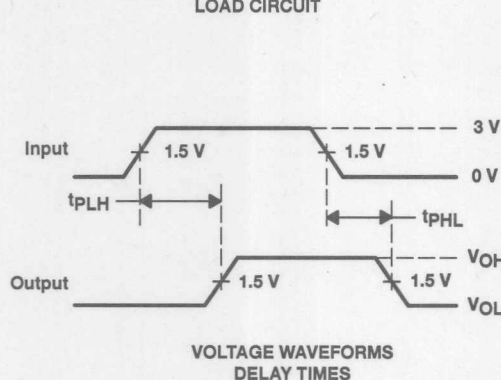
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# PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VCC
tPHZ/tPZH	GND



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
D. The outputs are measured one at a time with one input transition per measurement.

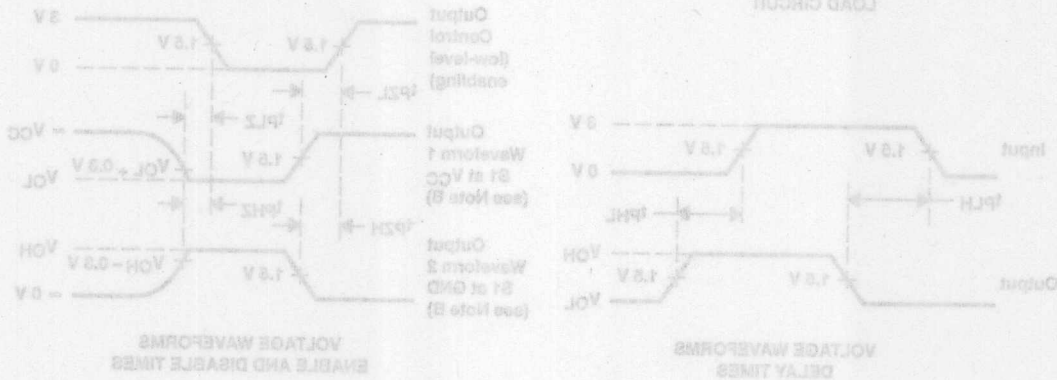
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

TEST	SI
1. $t_{PLH}$ , $t_{PHL}$	Open
2. $t_{PLZ}$ , $t_{PHZ}$	VCC
3. $t_{PLZ}$ , $t_{PHZ}$	GND



LOAD CIRCUIT



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $V_L = 3$  V,  $t_r = 5$  ns. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# SN74AHCT244 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

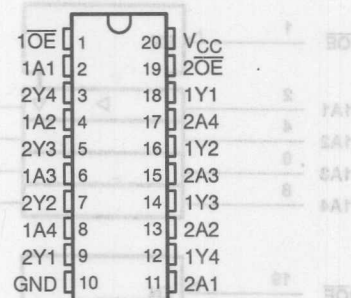
## description

This octal buffer/driver is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74AHCT244 is organized as two 4-bit buffers/line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The SN74AHCT244 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, $V_{CC}$	0 V to 5.0 V
Input voltage range, $V_I$ (see Note 1)	0 V to 5.0 V
Output voltage range, $V_O$ (see Note 1)	0 V to 5.0 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	25 mA
Continuous current through $V_{CC}$ or GND	25 mA
Maximum power dissipation at $T_A = 55^{\circ}\text{C}$ (in still air) (see Note 2)	0.8 W
	1.8 W
	1.8 W
	0.7 W
Storage temperature range, $T_{stg}$	$-85^{\circ}\text{C}$ to $150^{\circ}\text{C}$

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage range may be exceeded if the input and output current ratings are observed.

2. The maximum power dissipation is calculated using a junction temperature of  $100^{\circ}\text{C}$  and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

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PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

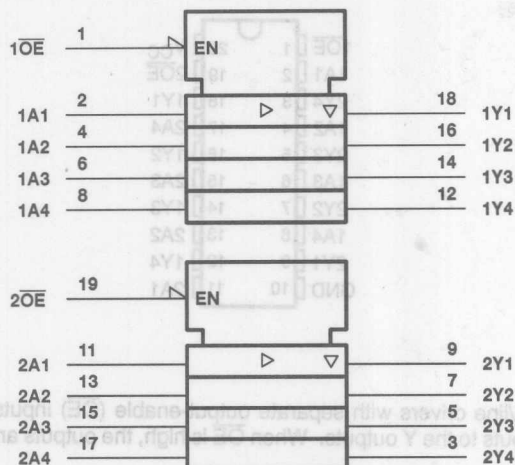
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# **SN74AHCT244** **OCTAL BUFFER/DRIVER** **WITH 3-STATE OUTPUTS**

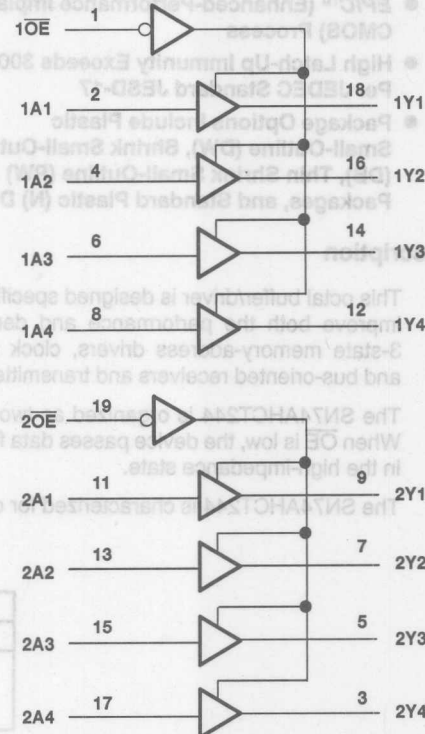
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



FUNCTION TABLE  
(each buffer)

OUTPUT Y	INPUTS A	OE
H	H	L
L	L	L
X	X	H

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	-20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	$\pm 75$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	-65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.



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# SN74AHCT244 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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## recommended operating conditions(see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-8	mA
$I_{OL}$	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	4.5 V	3.15	3.65		3.15		V
	$I_{OH} = -8\ \text{mA}$		2.5			2.4		
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	4.5 V			0.1		0.1	V
	$I_{OL} = 8\ \text{mA}$				0.36		0.44	
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.5 V			$\pm 0.25$		$\pm 2.5$	$\mu\text{A}$
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40	$\mu\text{A}$
$\Delta I_{CC}^\dagger$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			1.35		1.5	mA
$I_{off}$	$V_O = 5.5\ \text{V}$	0 V			0.5		5	$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	5 V			2.5		10	pF
$C_o$	$V_O = V_{CC}$ or GND	5 V			3			pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .



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**SN74AHCT244**  
**OCTAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended operating free-air temperature range  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	5.4	7.4	1	8.5	ns	
t <sub>PHL</sub>				5.4	7.4	1	8.5		
t <sub>PZH</sub>	OE	Y		7.7	10.4	1	12	ns	
t <sub>PZL</sub>				7.7	10.4	1	12		
t <sub>PHZ</sub>	OE	Y		5	9.4	1	10	ns	
t <sub>PLZ</sub>				5	9.4	1	10		
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	5.9	8.4	1	9.5	ns	
t <sub>PHL</sub>				5.9	8.4	1	9.5		
t <sub>PZH</sub>	OE	Y		8.2	11.4	1	13	ns	
t <sub>PZL</sub>				8.2	11.4	1	13		
t <sub>PHZ</sub>	OE	Y		8.8	11.4	1	13	ns	
t <sub>PLZ</sub>				8.8	11.4	1	13		

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER	$V_{CC}$	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_{sk(o)}$ Output skew	$5\text{ V} \pm 0.5\text{ V}$	1	1	1	1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.7		V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.7		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ ,	$f = 1\text{ MHz}$	8.2	pF

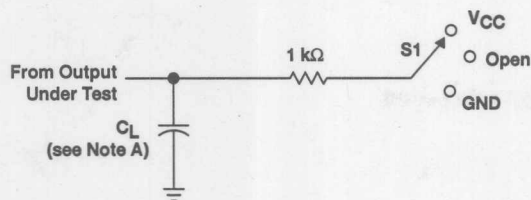


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# SN74AHCT244 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

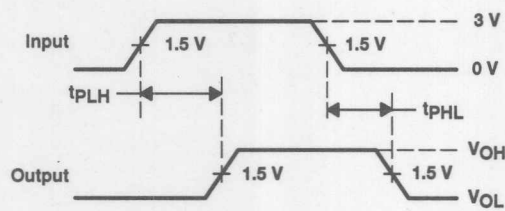
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## PARAMETER MEASUREMENT INFORMATION

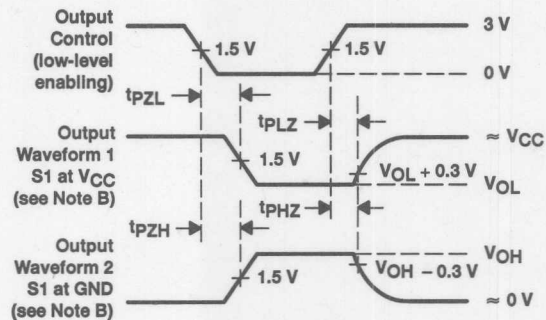


LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	VCC
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

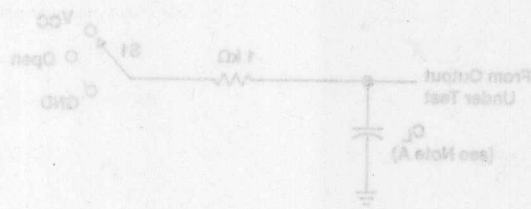
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

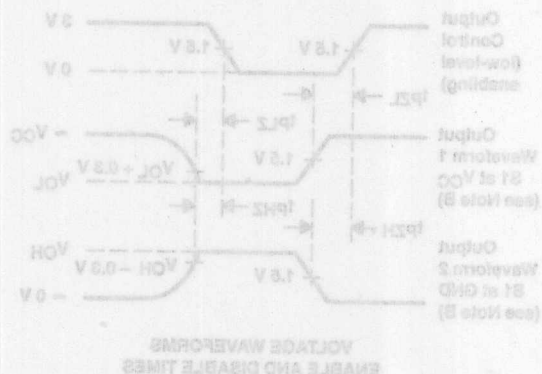


PARAMETER MEASUREMENT INFORMATION

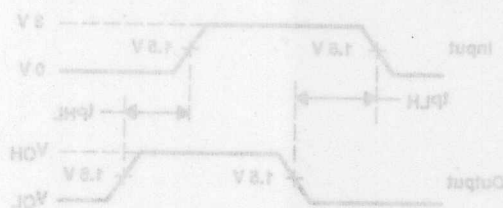
TEST	SI
1pLH/1pHL	Open
1pLZ/1pZL	VCC
1pHZ/1pZH	GND



LOAD CIRCUIT



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS  
DELAY TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $V = 3$  ns,  $t_r = 3$  ns.  
E. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# SN74AHCT245

## OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCLS233A – OCTOBER 1995 – REVISED FEBRUARY 1996

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 300 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

### description

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

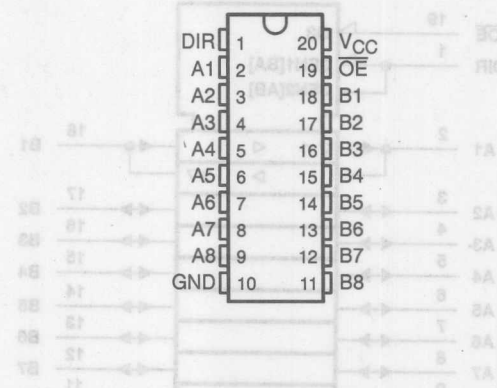
The SN74AHCT245 allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

The SN74AHCT245 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



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PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



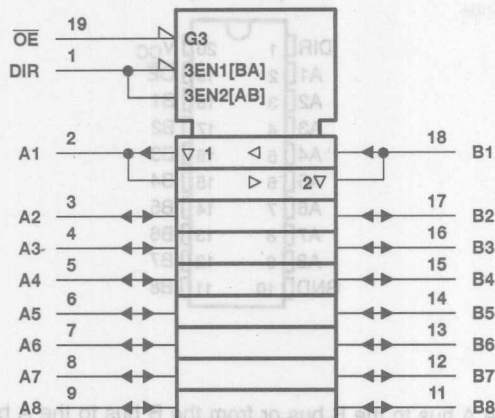
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# SN74AHCT245 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

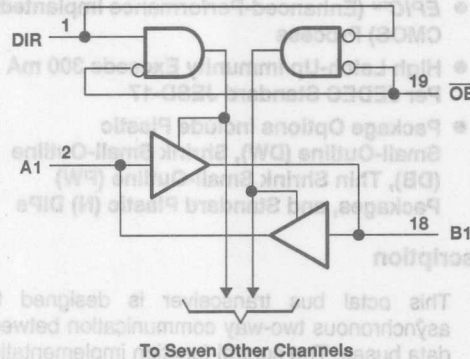
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	–20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.



# SN74AHCT245

## OCTAL BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-8	mA
I <sub>OL</sub>	Low-level output current		8	mA
Δt/Δv	Input transition rise or fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	3.15	3.65		3.15		V
	I <sub>OH</sub> = -8 mA		2.5			2.4		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 8 mA				0.36		0.44	
I <sub>OZ</sub>	A or B inputs† V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5	μA
I <sub>I</sub>	OE or DIR V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	μA
ΔI <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
I <sub>off</sub>	V <sub>O</sub> = 5.5 V	0 V			0.5		5	μA
C <sub>i</sub>	OE or DIR V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5	10		10	pF
C <sub>io</sub>	A or B inputs V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4				pF

† For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

PARAMETER	TEST CONDITIONS	TYP	UNIT
Power dissipation per transceiver	C <sub>I</sub> = 50 pF, f = 1 MHz	13	mW



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# SN74AHCT245

## OCTAL BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	B or A	C <sub>L</sub> = 15 pF	4.5	7.7	1	8.5	ns	
t <sub>PHL</sub>				4.5	7.7	1	8.5		
t <sub>PZH</sub>	OE	A or B	C <sub>L</sub> = 15 pF	8.9	13.8	1	15	ns	
t <sub>PZL</sub>				8.9	13.8	1	15		
t <sub>PHZ</sub>	OE	A or B	C <sub>L</sub> = 15 pF	9.2	14.4	1	15.5	ns	
t <sub>PLZ</sub>				9.2	14.4	1	15.5		
t <sub>PLH</sub>	A or B	B or A	C <sub>L</sub> = 50 pF	5.3	8.7	1	9.5	ns	
t <sub>PHL</sub>				5.3	8.7	1	9.5		
t <sub>PZH</sub>	OE	A or B	C <sub>L</sub> = 50 pF	9.7	14.8	1	16	ns	
t <sub>PZL</sub>				9.7	14.8	1	16		
t <sub>PHZ</sub>	OE	A or B	C <sub>L</sub> = 50 pF	10	15.4	1	16.5	ns	
t <sub>PLZ</sub>				10	15.4	1	16.5		

output-skew characteristics,  $C_L = 50\text{ pF}$  (see Note 4)

PARAMETER	$V_{CC}$	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_{sk(o)}$ Output skew	$5\text{ V} \pm 0.5\text{ V}$		1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		4		V
$V_{IH(D)}$ High-level dynamic input voltage	2			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

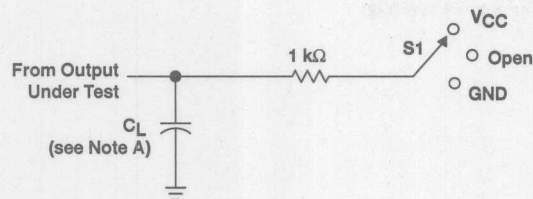
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per transceiver	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	13	pF



# SN74AHCT245 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

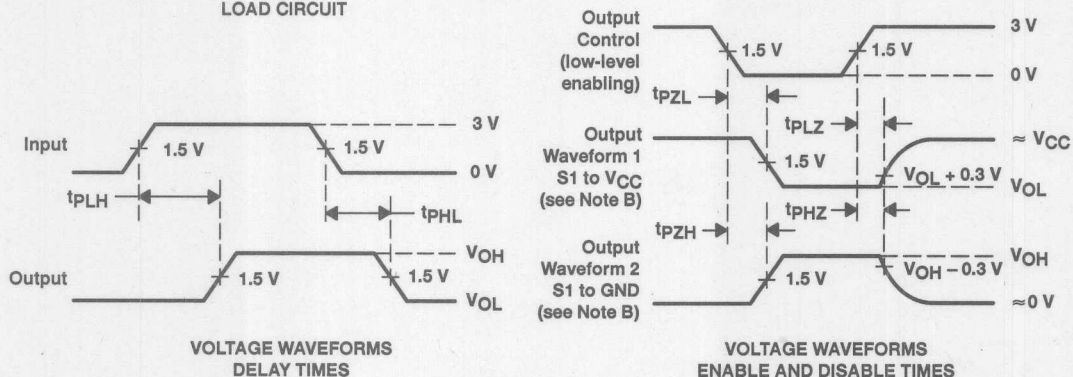
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## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>CC</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

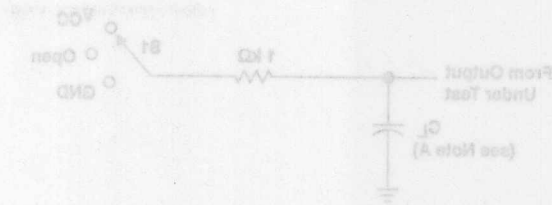


- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.
  - The outputs are measured one at a time with one input transition per measurement.

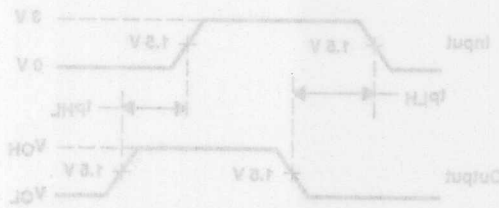
Figure 1. Load Circuit and Voltage Waveforms

# PARAMETER MEASUREMENT INFORMATION

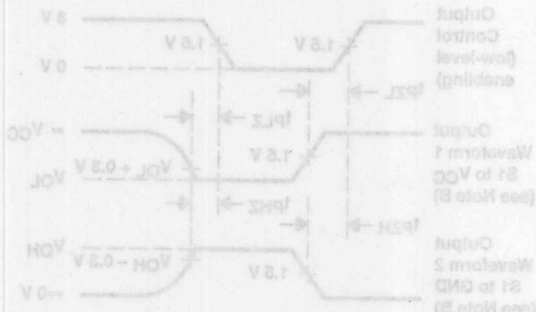
TEST	SI
$t_{PLH}/t_{PHL}$	Open
$t_{RZL}/t_{RZH}$	VCC
$t_{FZL}/t_{FZH}$	GND



## LOAD CIRCUIT



## VOLTAGE WAVEFORMS DELAY TIMES



## VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

- NOTE: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
E. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

# SN74AHCT373

## OCTAL TRANSPARENT D-TYPE LATCH

### WITH 3-STATE OUTPUTS

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- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

#### description

The SN74AHCT373 is an octal-transparent D-type latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

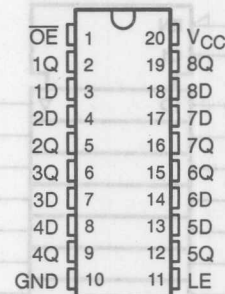
$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHCT373 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

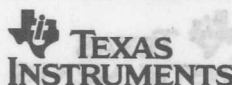
DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



TEST	MAX	MIN
V <sub>CC</sub>	5.5	4.5
V <sub>OH</sub>	2	
V <sub>IL</sub>	0.8	
V <sub>I</sub>	0	0
V <sub>O</sub>	0	0
I <sub>OH</sub>	8	
I <sub>OL</sub>	8	
t <sub>PLH</sub>	20	
t <sub>PHL</sub>	20	
T <sub>A</sub>	85	-40

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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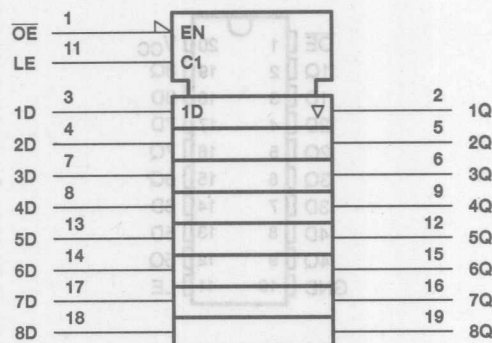
# SN74AHCT373

## OCTAL TRANSPARENT D-TYPE LATCH

### WITH 3-STATE OUTPUTS

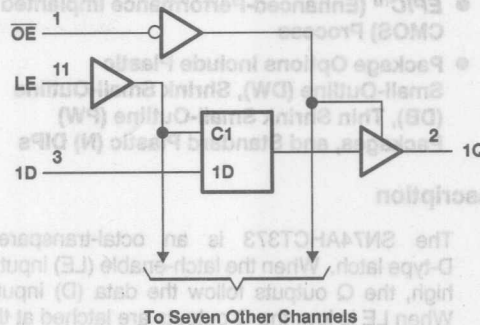
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#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	−0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	−0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	−0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	−20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	−20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air)(see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

#### recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		V
$V_{IL}$ Low-level input voltage		0.8	V
$V_I$ Input voltage	0	$V_{CC}$	V
$V_O$ Output voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current		−8	mA
$I_{OL}$ Low-level output current		8	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		20	ns/V
$T_A$ Operating free-air temperature	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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**SN74AHCT373**  
**OCTAL TRANSPARENT D-TYPE LATCH**  
**WITH 3-STATE OUTPUTS**  
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	4.5 V	3.15	3.65		3.15		V
	I <sub>OH</sub> = -8 mA		2.5			2.4		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 8 mA				0.36		0.44	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			± 0.25		± 2.5	µA
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			± 0.1		± 1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	µA
ΔI <sub>CC</sub> <sup>†</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
I <sub>off</sub>	V <sub>O</sub> = 5.5 V	0 V			0.5		5	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			4			pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V			6			pF

<sup>†</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

timing requirements over recommended operating free-air temperature range,  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t <sub>w</sub>	Pulse duration, $\overline{LE}$ high	5		5		ns
t <sub>su</sub>	Setup time, data before $\overline{LE}\downarrow$	4		4		ns
t <sub>h</sub>	Hold time, data after $\overline{LE}\downarrow$	1		1		ns

switching characteristics over recommended free-air temperature operating range,  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
				MIN	MAX			
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 15 pF	7.2	1	8.5	ns	
t <sub>PHL</sub>				7.2	1	8.5		
t <sub>PLH</sub>	LE	Q		7.2	1	8.5	ns	
t <sub>PHL</sub>				7.2	1	8.5		
t <sub>PZH</sub>	$\overline{OE}$	Q		8.1	1	9.5	ns	
t <sub>PZL</sub>				8.1	1	9.5		
t <sub>PHZ</sub>	$\overline{OE}$	Q					ns	
t <sub>PLZ</sub>								
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 50 pF	9.2	1	10.5	ns	
t <sub>PHL</sub>				9.2	1	10.5		
t <sub>PLH</sub>	LE	Q		9.2	1	10.5	ns	
t <sub>PHL</sub>				9.2	1	10.5		
t <sub>PZH</sub>	$\overline{OE}$	Q		10.1	1	11.5	ns	
t <sub>PZL</sub>				10.1	1	11.5		
t <sub>PHZ</sub>	$\overline{OE}$	Q		9.2	1	10.5	ns	
t <sub>PLZ</sub>				9.2	1	10.5		

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noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

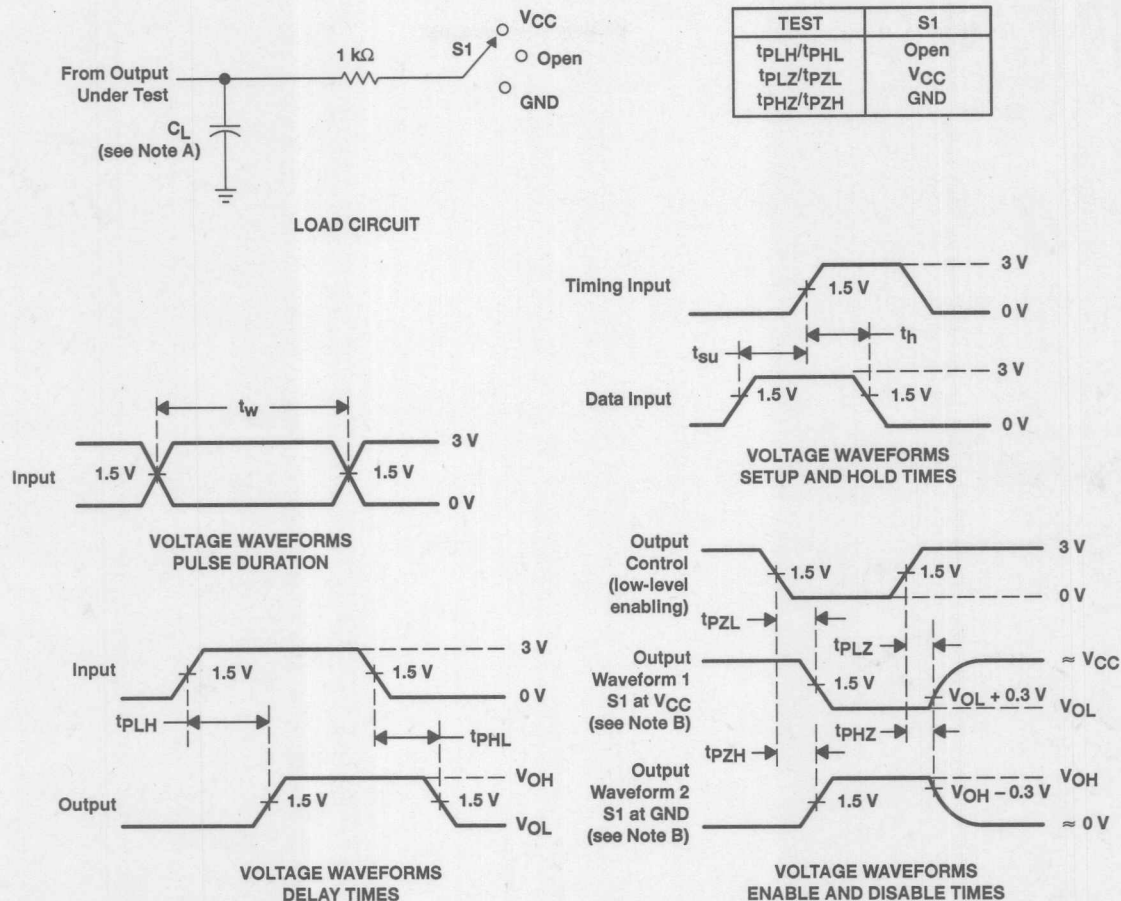
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

# SN74AHCT373 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.
  - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



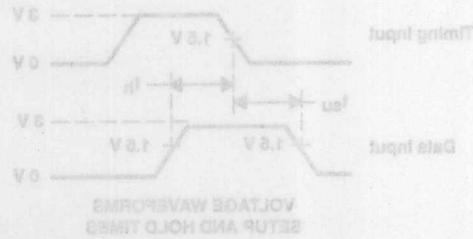
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PARAMETER MEASUREMENT INFORMATION

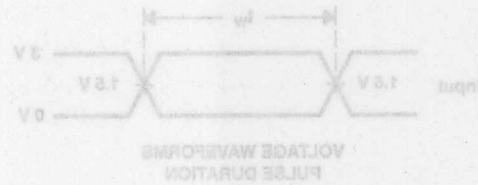
TEST	SI
PLH/PHL	Open
PLZ/PSL	VCC
PHZ/PSH	GND



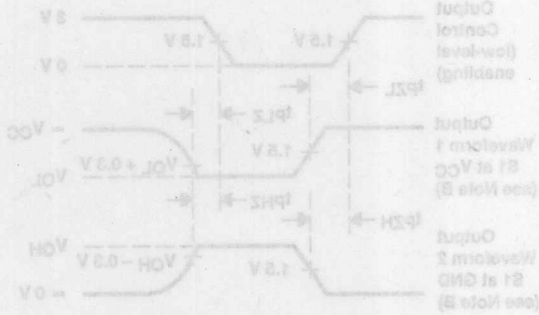
LOAD CIRCUIT



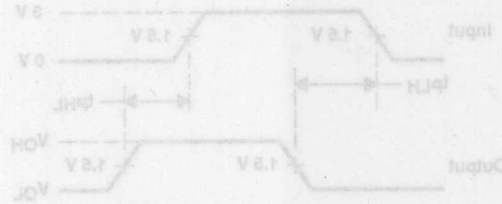
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS  
DELAY TIMES

- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_0 = 50 \Omega$ ,  $V = 3$  V,  $t_r = 3$  ns.  
E. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW



# SN74AHCT374

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCLS241—OCTOBER 1995

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

### description

The SN74AHCT374 is an octal edge-triggered D-type flip-flop that features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

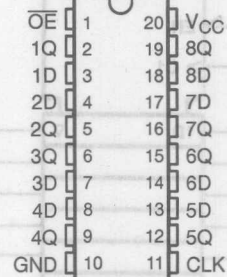
On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHCT374 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	H or L	X	$Q_0$
H	X	X	Z

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**TEXAS  
INSTRUMENTS**

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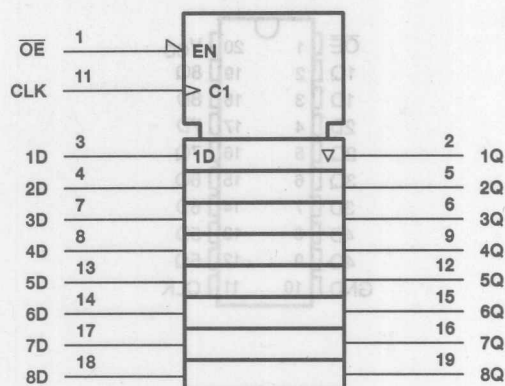
PRODUCT PREVIEW

# SN74AHCT374

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

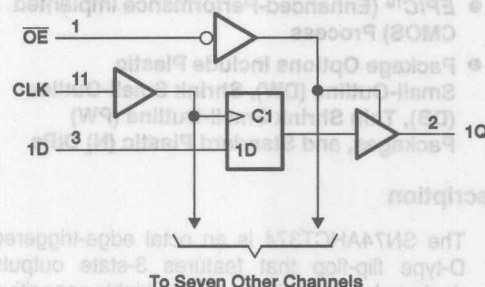
SCLS241 – OCTOBER 1995

### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



To Seven Other Channels

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	–20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

PRODUCT PREVIEW



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**SN74AHCT374**  
**OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**  
SCLS241 – OCTOBER 1995

**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-8	mA
I <sub>OL</sub>	Low-level output current		8	mA
Δt/Δv	Input transition rise or fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	3.15	3.65		3.15		V
	I <sub>OH</sub> = -8 mA		2.5			2.4		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 8 mA				0.36		0.44	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	5.5 V		±0.25		±2.5		μA
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		±0.1		±1		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	μA
ΔI <sub>CC</sub> †	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
I <sub>off</sub>	V <sub>O</sub> = 5.5 V	0 V			0.5		5	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			4			pF
C <sub>O</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			6			pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted)(see Figure 1)**

		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t <sub>w</sub>	Pulse duration, CLK high or low	5		5		ns
t <sub>su</sub>	Setup time, data before CLK↑	5		5.5		ns
t <sub>h</sub>	Hold time, data after CLK↑	1.5		1.5		ns

PRODUCT PREVIEW



**SN74AHCT374**  
**OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted)(see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
				MIN	TYP	MAX				
f <sub>max</sub>			C <sub>L</sub> = 15 pF	130			110		MHz	
			C <sub>L</sub> = 50 pF	85			75			
t <sub>PLH</sub>	CLK	Q	C <sub>L</sub> = 15 pF	8.1			1	9.5	ns	
t <sub>PHL</sub>				8.1			1	9.5		
t <sub>PZH</sub>	OE	Q		C <sub>L</sub> = 15 pF	7.6			1	9	ns
t <sub>PZL</sub>					7.6			1	9	
t <sub>PHZ</sub>	OE	Q	C <sub>L</sub> = 50 pF							ns
t <sub>PLZ</sub>										
t <sub>PLH</sub>	CLK	Q		10.1			1	11.5	ns	
t <sub>PHL</sub>				10.1			1	11.5		
t <sub>PZH</sub>	OE	Q		9.6			1	11	ns	
t <sub>PZL</sub>				9.6			1	11		
t <sub>PHZ</sub>	OE	Q		8.8			1	10	ns	
t <sub>PLZ</sub>				8.8			1	10		

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

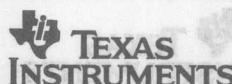
NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$			40		pF

UNIT	MAX	MIN	$T_A = 25^\circ\text{C}$	
			MAX	MIN
ns	5	5		
ns	5.5	5		
ns	1.5	1.5		

PRODUCT PREVIEW



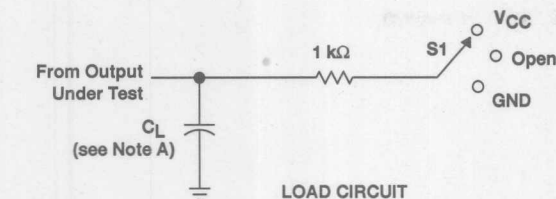
# SN74AHCT374

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP

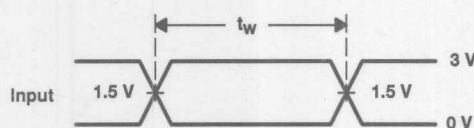
### WITH 3-STATE OUTPUTS

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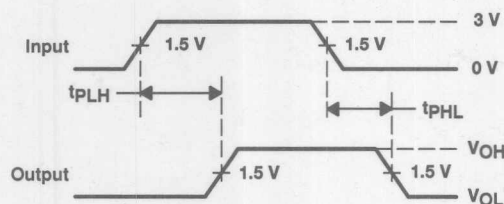
#### PARAMETER MEASUREMENT INFORMATION



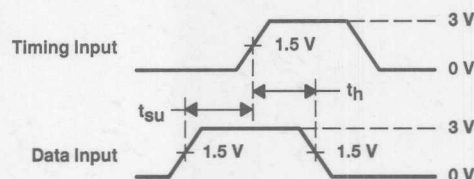
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	VCC
$t_{PHZ}/t_{PZH}$	GND



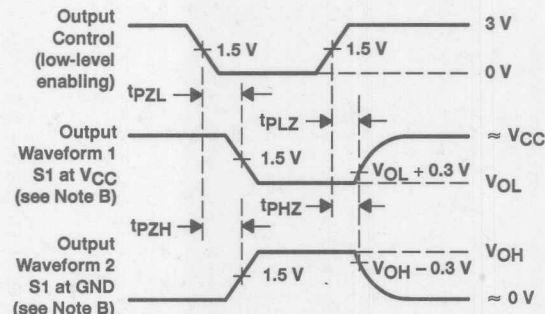
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
DELAY TIMES



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.

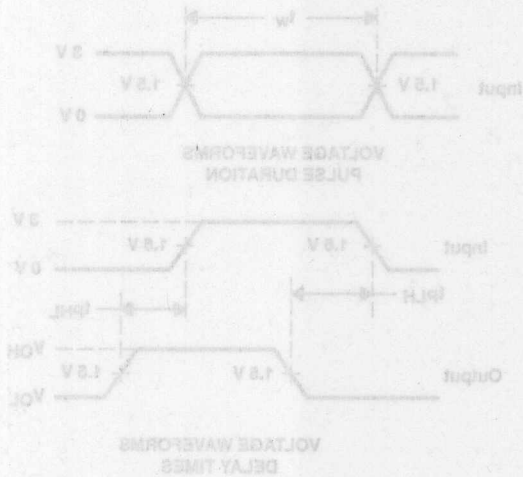
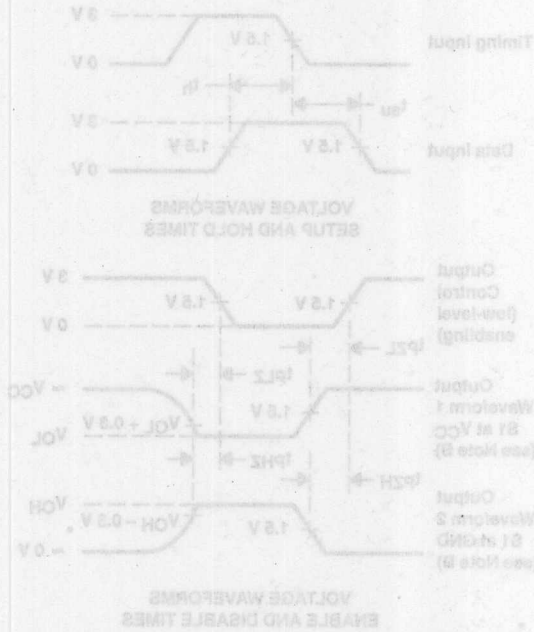
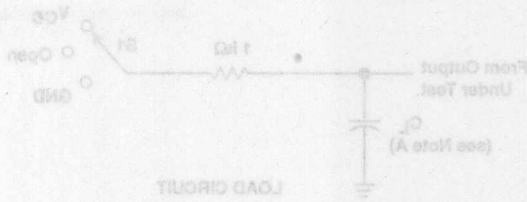
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW



PARAMETER MEASUREMENT INFORMATION

TEST	SI
1PHZ/PHL	Open
1PHZ/PXL	VCC
1PHZ/PLN	GND



NOTES:  
A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $V = 3$  V.  
E. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

WAVEFORM REVIEW

# SN74AHCT540

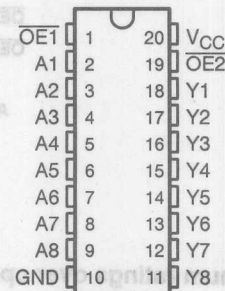
## OCTAL BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

SCLS268 - DECEMBER 1995

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



### description

The SN74AHCT540 octal buffer/driver is ideal for driving bus lines or buffer memory address registers. This device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

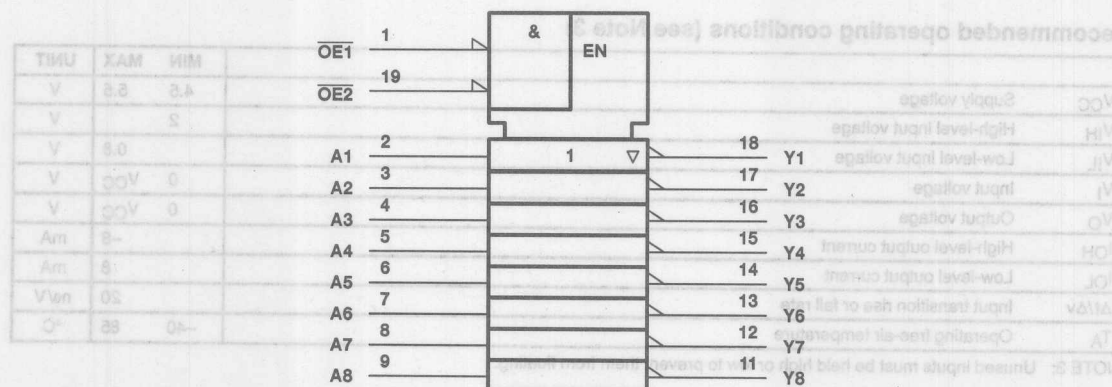
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

The SN74AHCT540 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

### logic symbol



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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**TEXAS**  
**INSTRUMENTS**

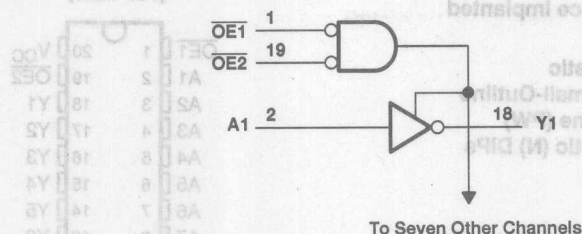
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# SN74AHCT540 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCLS268 - DECEMBER 1995

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	–20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–8	mA
$I_{OL}$	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	4.5 V	3.15	3.65		3.15		V
	I <sub>OH</sub> = -8 mA		2.5			2.4		V
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 8 mA				0.36		0.44	V
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5	µA
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	µA
ΔI <sub>CC</sub> <sup>†</sup>	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V			1.35		1.5	mA
I <sub>off</sub>	V <sub>O</sub> = 5.5 V	0 V			0.5		5	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			4		10	pF
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V			9			pF

<sup>†</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF						ns
t <sub>PHL</sub>									
t <sub>PZH</sub>	OE	Y	C <sub>L</sub> = 15 pF						ns
t <sub>PZL</sub>									
t <sub>PHZ</sub>	OE	Y	C <sub>L</sub> = 15 pF						ns
t <sub>PLZ</sub>									
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF						ns
t <sub>PHL</sub>									
t <sub>PZH</sub>	OE	Y	C <sub>L</sub> = 50 pF						ns
t <sub>PZL</sub>									
t <sub>PHZ</sub>	OE	Y	C <sub>L</sub> = 50 pF						ns
t <sub>PLZ</sub>									

output-skew characteristics, C<sub>L</sub> = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>sk(o)</sub>	A	Y	5 V ± 0.5 V			1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

PRODUCT PREVIEW



# SN74AHCT540

## OCTAL BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

SCLS268 – DECEMBER 1995

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

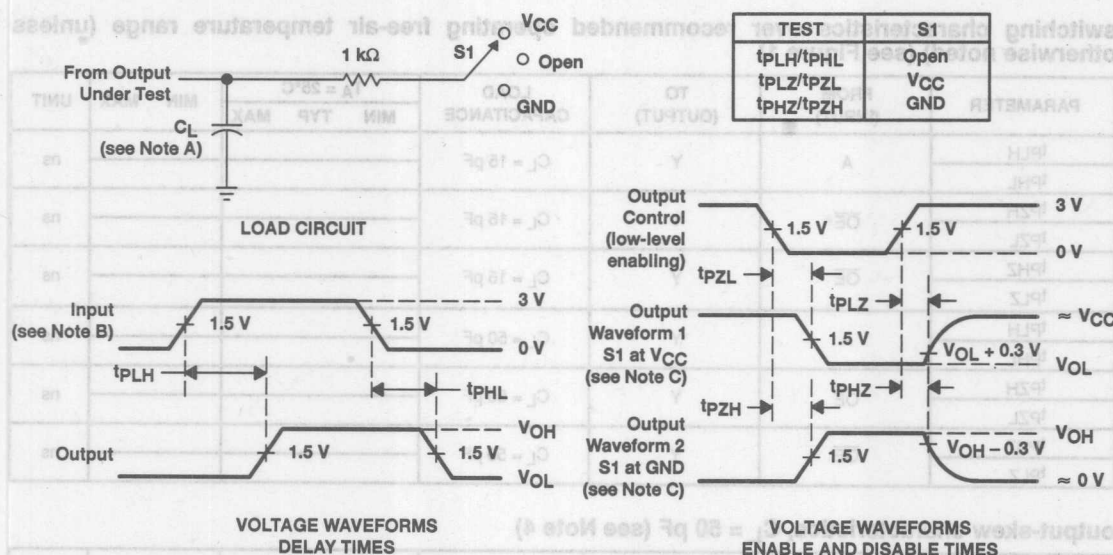
PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$ High-level dynamic input voltage	Am	2		V
$V_{IL(D)}$ Low-level dynamic input voltage	Am		0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$		pF

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



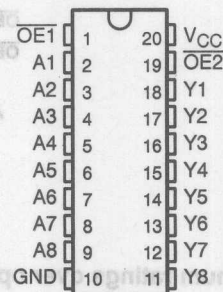


# SN74AHCT541 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCLS269B – DECEMBER 1995 – REVISED JANUARY 1996

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



## description

The SN74AHCT541 octal buffer/driver is ideal for driving bus lines or buffer memory address registers. This device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

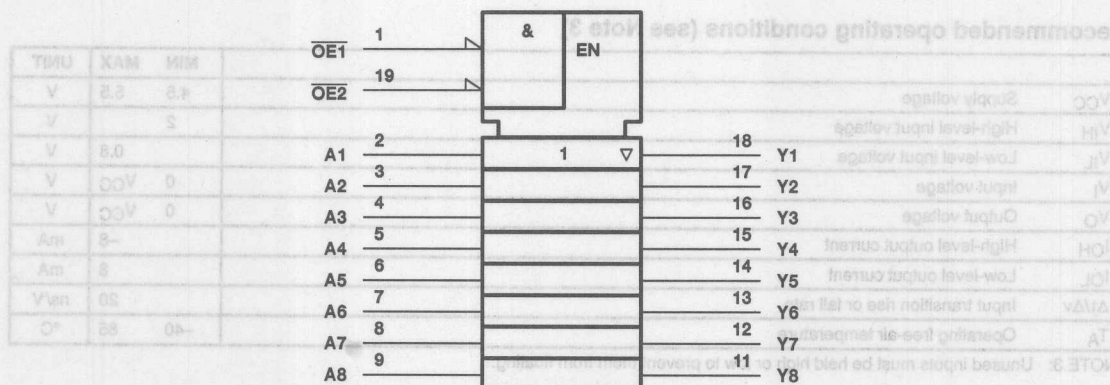
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

The SN74AHCT541 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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**logic diagram (positive logic)**



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	-20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 75$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air)(see Note 2): DB package .....	0.6 W

Storage temperature range,  $T_{\text{stg}}$  .....  $-65^{\circ}\text{C}$  to  $150^{\circ}\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		−8	mA
I <sub>OL</sub>	Low-level output current		8	mA
Δt/Δv	Input transition rise or fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

**SN74AHCT541**  
**OCTAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	4.5 V	3.15	3.65		3.15		V
	I <sub>OH</sub> = -8 mA		2.5			2.4		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 8 mA				0.36		0.44	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5	µA
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	µA
ΔI <sub>CC</sub> <sup>†</sup>	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V			1.35		1.5	mA
I <sub>off</sub>	V <sub>O</sub> = 5.5 V	0 V			0.5		5	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10		10	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		9				pF

<sup>†</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

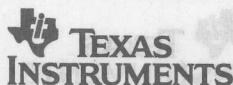
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF						ns
t <sub>PHL</sub>									
t <sub>PZH</sub>	OE	Y	C <sub>L</sub> = 15 pF						ns
t <sub>PZL</sub>									
t <sub>PHZ</sub>	OE	Y	C <sub>L</sub> = 15 pF						ns
t <sub>PLZ</sub>									
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF						ns
t <sub>PHL</sub>									
t <sub>PZH</sub>	OE	Y	C <sub>L</sub> = 50 pF						ns
t <sub>PZL</sub>									
t <sub>PHZ</sub>	OE	Y	C <sub>L</sub> = 50 pF						ns
t <sub>PLZ</sub>									

output-skew characteristics, C<sub>L</sub> = 50 pF (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>sk(o)</sub>	A	Y	5 V ± 0.5 V			1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

PRODUCT PREVIEW



# SN74AHCT541 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

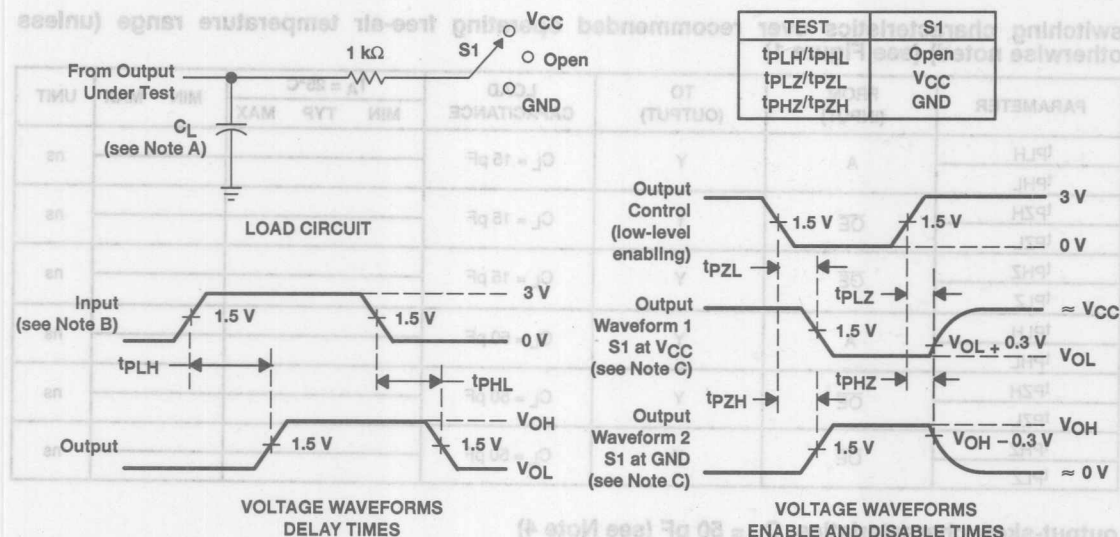
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$		pF

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





# SN74AHCT573 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCLS243B - OCTOBER 1995 - REVISED JANUARY 1996

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

## description

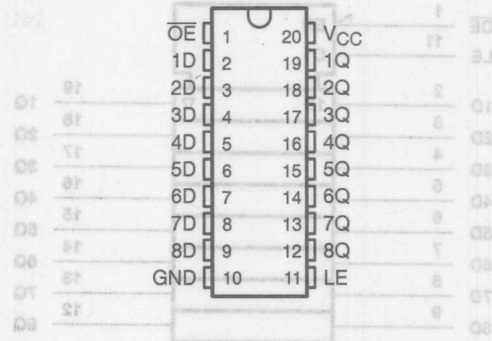
The SN74AHCT573 is an octal-transparent D-type latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHCT573 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

TEST	MAX	MIN	UNIT
V <sub>CC</sub>	5.5	4.5	V
V <sub>IL</sub>	0.8	0	V
V <sub>OL</sub>	0.1	0	V
I <sub>IL</sub>	0	0	mA
I <sub>OL</sub>	0	0	mA
t <sub>PLH</sub>	20	20	ns
t <sub>PHL</sub>	20	20	ns
t <sub>tr</sub>	20	20	ns
t <sub>fall</sub>	20	20	ns
t <sub>rise</sub>	20	20	ns
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t <sub>delay</sub>	20	20	ns
t <sub>prop</sub>	20	20	ns
t <sub>setup</sub>	20	20	ns
t <sub>hold</sub>	20	20	ns
t <sub>delay</sub>	20	20	ns
t <sub>prop</sub>	20	20	ns
t <sub>setup</sub>	20	20	ns
t <sub>hold</sub>	20	20	ns
t <sub>delay</sub>	20	20	ns
t <sub>prop</sub>	20	20	ns
t <sub>setup</sub>	20	20	ns
t <sub>hold</sub>	20	20	ns
t <sub>delay</sub>	20	20	ns
t <sub>prop</sub>	20	20	ns

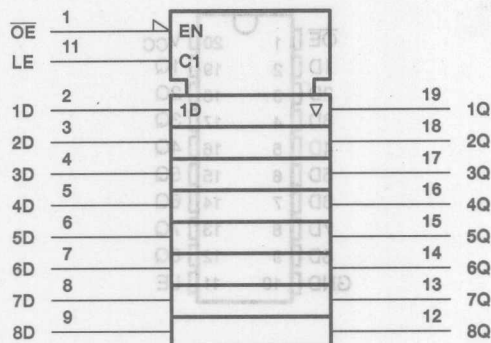


# SN74AHCT573

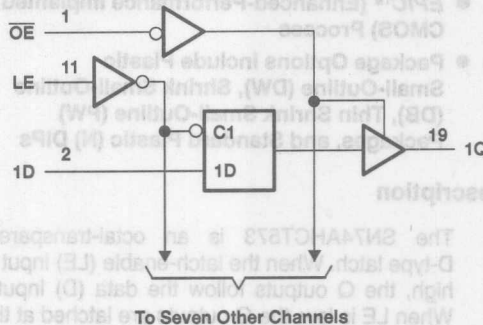
## OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCLS243B - OCTOBER 1995 - REVISED JANUARY 1996

### logic symbol†



### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	-20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	$\pm 75$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	-65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

### recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		V
$V_{IL}$ Low-level input voltage		0.8	V
$V_I$ Input voltage	0	$V_{CC}$	V
$V_O$ Output voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current		-8	mA
$I_{OL}$ Low-level output current		8	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		20	ns/V
$T_A$ Operating free-air temperature	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW



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**SN74AHCT573**  
**OCTAL TRANSPARENT D-TYPE LATCH**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = –50 µA	4.5 V	3.15	3.65		3.15		V
	I <sub>OH</sub> = –8 mA		2.5			2.4		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 8 mA				0.36		0.44	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5	µA
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	µA
ΔI <sub>CC</sub> <sup>†</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
I <sub>off</sub>	V <sub>O</sub> = 5.5 V	0 V			0.5		5	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			4		10	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V			6			pF

<sup>†</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t <sub>w</sub>	Pulse duration, $\overline{LE}$ high	5		5		ns
t <sub>su</sub>	Setup time, data before $\overline{LE}\downarrow$	3.5		3.5		ns
t <sub>h</sub>	Hold time, data after $\overline{LE}\downarrow$	1.5		1.5		ns

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
				MIN	MAX			
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 15 pF	6.8		1	8	ns
t <sub>PHL</sub>				6.8		1	8	
t <sub>PLH</sub>	LE	Q		7.7		1	9	ns
t <sub>PHL</sub>				7.7		1	9	
t <sub>PZH</sub>	OE	Q		7.7		1	9	ns
t <sub>PZL</sub>				7.7		1	9	
t <sub>PHZ</sub>	OE	Q						ns
t <sub>PLZ</sub>								
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 50 pF	8.8		1	10	ns
t <sub>PHL</sub>				8.8		1	10	
t <sub>PLH</sub>	LE	Q		9.7		1	11	ns
t <sub>PHL</sub>				9.7		1	11	
t <sub>PZH</sub>	OE	Q		9.7		1	11	ns
t <sub>PZL</sub>				9.7		1	11	
t <sub>PHZ</sub>	OE	Q		9.7		1	11	ns
t <sub>PLZ</sub>				9.7		1	11	

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# SN74AHCT573 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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output-skew characteristics,  $C_L = 50$  pF (see Note 4)

UNIT	PARAMETER	$V_{CC}$	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
t <sub>sk(o)</sub>	Output skew	5 V ± 0.5 V	1		1		ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics,  $V_{CC} = 5$  V,  $C_L = 50$  pF,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>			0.8	V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>			-0.8	V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>				V
V <sub>IH(D)</sub>	High-level dynamic input voltage	2			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

operating characteristics,  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	$C_L = 50$ pF, $f = 1$ MHz		25	pF

PRODUCT PREVIEW

UNIT	MAX	MIN	$T_A = 25^\circ\text{C}$	
			MAX	MIN
ns	8	5	5	5
ns	3.5	3.5	3.5	3.5
ns	7.5	7.5	7.5	7.5

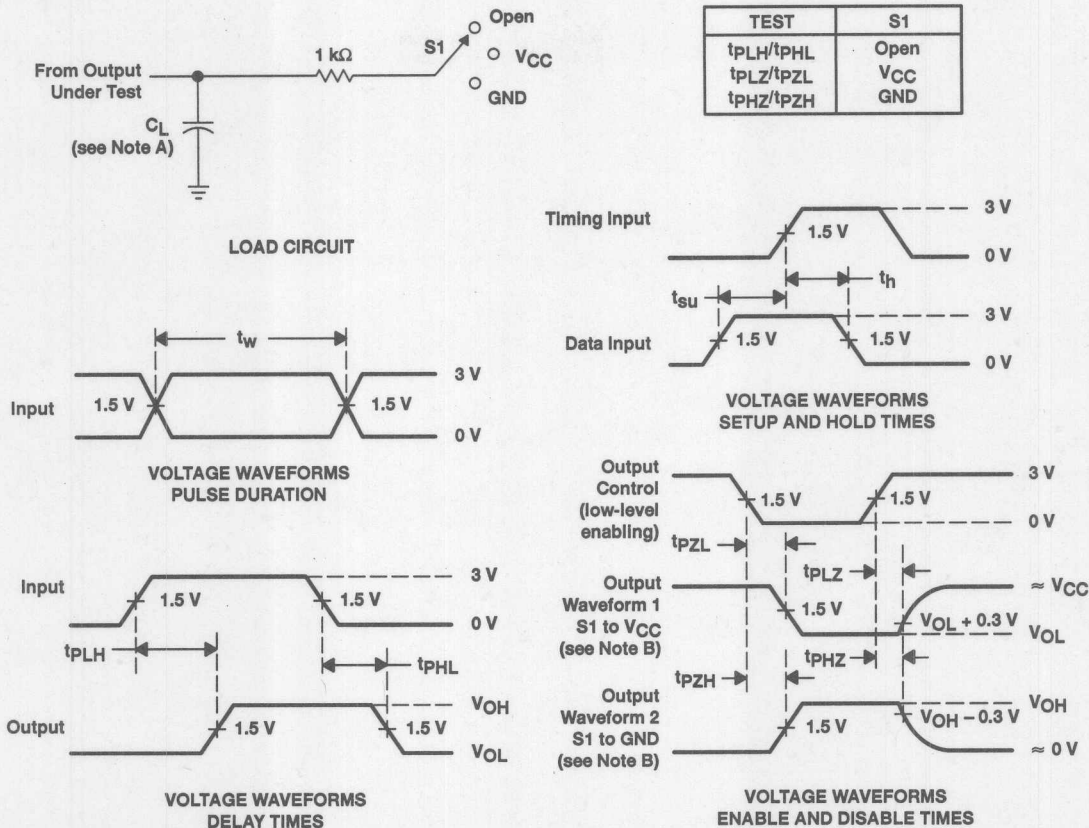
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$	
				MAX	MIN
t <sub>PLH</sub>	D	Q	$C_L = 50$ pF	8.5	7
t <sub>PLH</sub>	Q	Q		8.5	7
t <sub>PLH</sub>	LE	Q		7.7	7
t <sub>PLH</sub>	OE	Q		7.7	7
t <sub>PLH</sub>	OE	Q		7.7	7
t <sub>PLH</sub>	OE	Q		7.7	7
t <sub>PLH</sub>	Q	Q	$C_L = 50$ pF	8.5	7
t <sub>PLH</sub>	Q	Q		8.5	7
t <sub>PLH</sub>	LE	Q		8.7	7
t <sub>PLH</sub>	OE	Q		8.7	7
t <sub>PLH</sub>	OE	Q		8.7	7
t <sub>PLH</sub>	OE	Q		8.7	7



# SN74AHCT573 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION

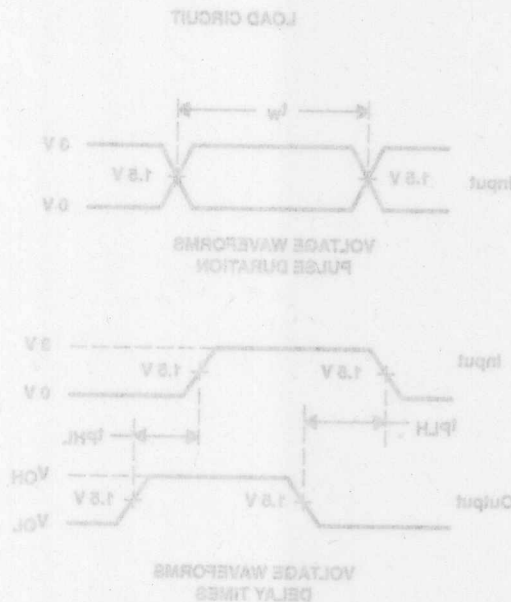
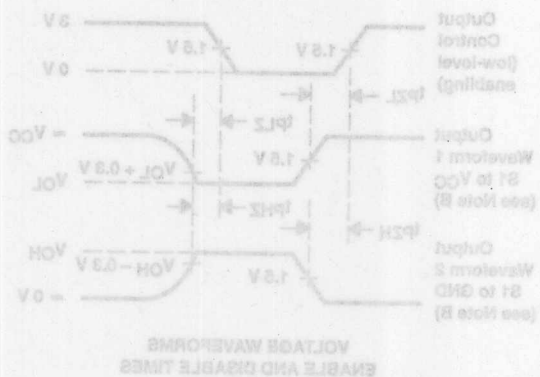
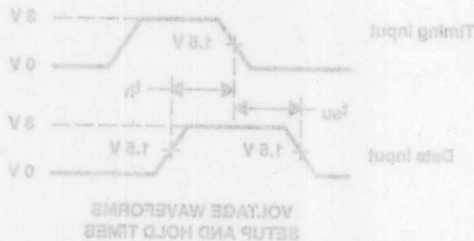
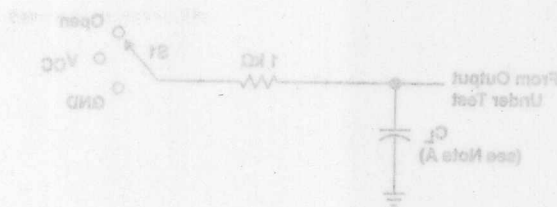


- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

TEST	SI
Input High	Open
Input Low	VCC
Output	GND



NOTES:  
A. CL includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. Waveform 2 is for an output with internal conditions such that the output is low except when disabled by the output control.  
D. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $t_r \leq 2$  ns,  $t_f \leq 2$  ns.  
E. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

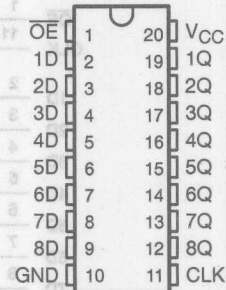


# SN74AHCT574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) DIPs

DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



## description

The SN74AHCT574 is an octal edge-triggered D-type flip-flop that features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74AHCT574 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L or H	X	$Q_0$
H	X	X	Z

PRODUCT PREVIEW

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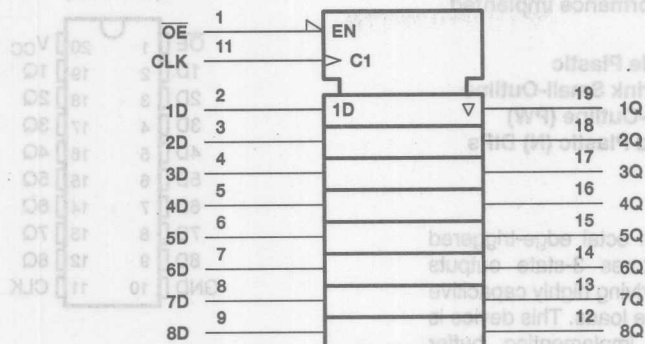
# SN74AHCT574

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP

### WITH 3-STATE OUTPUTS

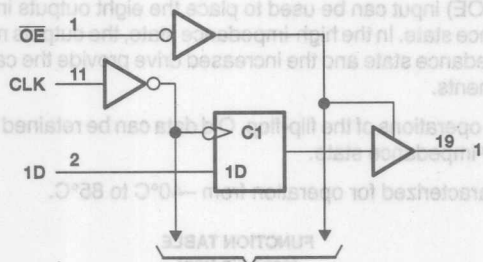
SCLS245 – OCTOBER 1995

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	–20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

**SN74AHCT574**  
**OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**  
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**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-8	mA
I <sub>OL</sub>	Low-level output current		8	mA
Δt/Δv	Input transition rise or fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	3.15	3.65		3.15		V
	I <sub>OH</sub> = -8 mA		2.5			2.4		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 8 mA				0.36		0.44	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5	μA
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	μA
ΔI <sub>CC</sub> †	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
I <sub>off</sub>	V <sub>O</sub> = 5.5 V	0 V			0.5		5	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4.5				pF
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		15				pF

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

V		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t <sub>w</sub>	Pulse duration, CLK high or low	5		5.5		ns
t <sub>su</sub>	Setup time, data before CLK↑	3.5		3.5		ns
t <sub>h</sub>	Hold time, data after CLK↑	1.5		1.5		ns

PRODUCT PREVIEW



# **SN74AHCT574** **OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP** **WITH 3-STATE OUTPUTS**

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switching characteristics over recommended operating free-air temperature range,  
 **$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$**  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$f_{\text{max}}$			$C_L = 15\text{ pF}$	130	180		110		MHz
			$C_L = 50\text{ pF}$	85	115		75		
$t_{\text{PLH}}$	CLK	Q	$C_L = 15\text{ pF}$			8.6	1	10	ns
$t_{\text{PHL}}$						8.6	1	10	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	$C_L = 15\text{ pF}$			9	1	10.5	ns
$t_{\text{PZL}}$						9	1	10.5	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	$C_L = 15\text{ pF}$						ns
$t_{\text{PLZ}}$									
$t_{\text{PLH}}$	CLK	Q	$C_L = 50\text{ pF}$			10.6	1	12	ns
$t_{\text{PHL}}$						10.6	1	12	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	$C_L = 50\text{ pF}$			11	1	12.5	ns
$t_{\text{PZL}}$						11	1	12.5	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	$C_L = 50\text{ pF}$			10.1	1	11.5	ns
$t_{\text{PLZ}}$						10.1	1	11.5	

output-skew characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$   
(see Note 4)

PARAMETER	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
		MIN	TYP	MAX			
$t_{\text{sk(o)}}$ Output skew	$5\text{ V} \pm 0.5\text{ V}$			1		1	ns

NOTE 4: Characteristics are determined during product characterization and ensured by design.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$			0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$			-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$				V
$V_{IH(D)}$ High-level dynamic input voltage	2			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

NOTE 5: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

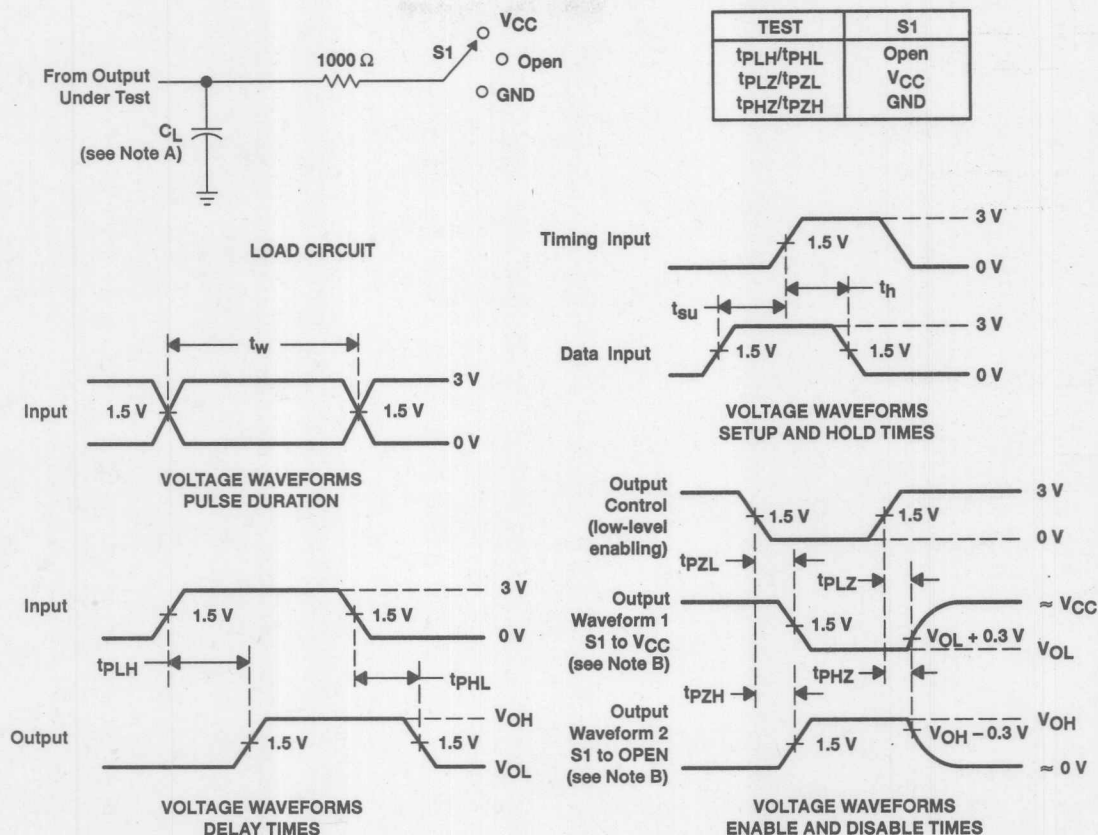
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	40	pF

PRODUCT PREVIEW



### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.

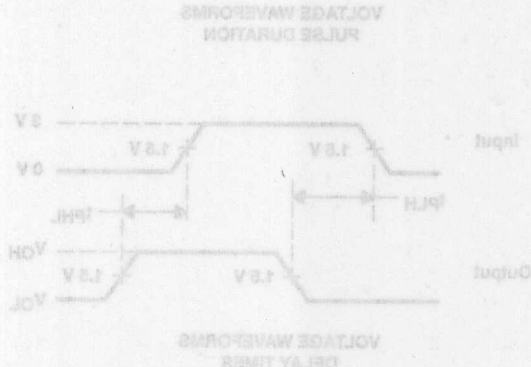
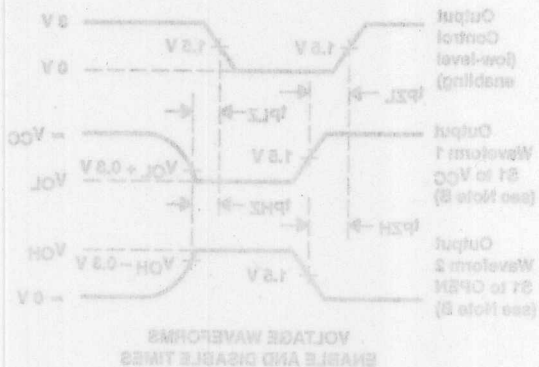
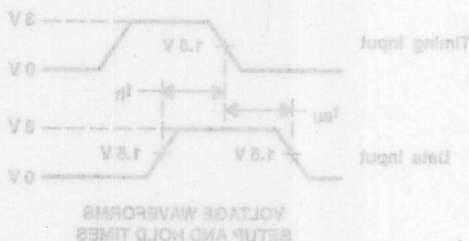
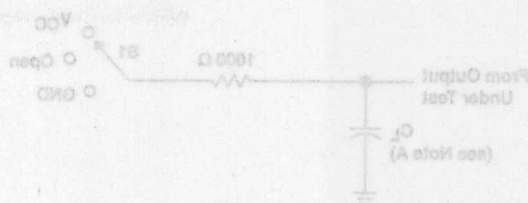
**Figure 1. Load Circuit and Voltage Waveforms**

**PRODUCT PREVIEW**



PARAMETER MEASUREMENT INFORMATION

TEST	SET
$t_{PLH}$ , $t_{PHL}$	Open
$t_{SLZ}$ , $t_{HIZ}$	VCC
$t_{FZL}$ , $t_{FZH}$	GND



- NOTES:  
 A. C1 includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR = 1 MHz,  $t_r = 10$  ns,  $t_f = 10$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

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## Mechanical Data

## ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: SN 74AHC244 DB LE

### Prefix

SN = Standard prefix

SNJ = MIL-STD-883 processed and screened per JEDEC Standard 101

### Unique Circuit Description

MUST CONTAIN SEVEN TO ELEVEN CHARACTERS

Examples: 74AHC00  
74AHCT245

### Package

MUST CONTAIN ONE TO THREE LETTERS

D, DW = plastic small-outline package

DB = plastic shrink small-outline package

N = plastic dual-in-line package

PW = plastic thin shrink small-outline package  
(from pin-connection diagram on individual data sheet)

### Tape and Reel Packaging

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

MUST CONTAIN ONE OR TWO LETTERS

LE = Left embossed tape and reel (required for DB and PW packages)

R = Standard tape and reel (optional for D and DW packages)



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# ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: SN T4AHCT24S DB LE

Prefix

SN = Standard prefix  
 SN1 = MIL-STD-883 processed and screened per JEDEC Standard 101

Unique Circuit Description

MUST CONTAIN SEVEN TO ELEVEN CHARACTERS

Examples: T4AHCT24S  
 T4AHCT00

Package

MUST CONTAIN ONE TO THREE LETTERS

D, DW = plastic small-outline package  
 DB = plastic shrink small-outline package  
 N = plastic dual-in-line package  
 PW = plastic thin shrink small-outline package  
 (from pin-connection diagram on individual data sheet)

Tape and Reel Packaging

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

MUST CONTAIN ONE OR TWO LETTERS

LE = Left embossed tape and reel (required for DB and PW packages)  
 R = Standard tape and reel (optional for D and DW packages)

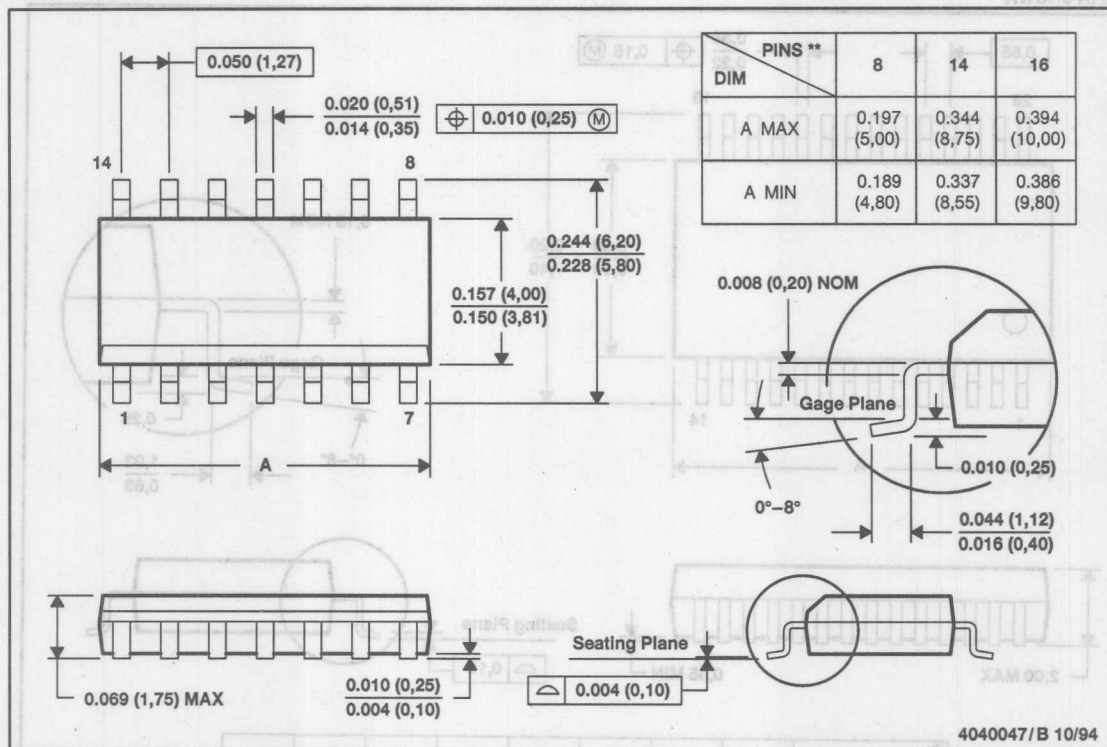


# MECHANICAL DATA

D (R-PDSO-G\*\*) PLASTIC SMALL-OUTLINE PACKAGE

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



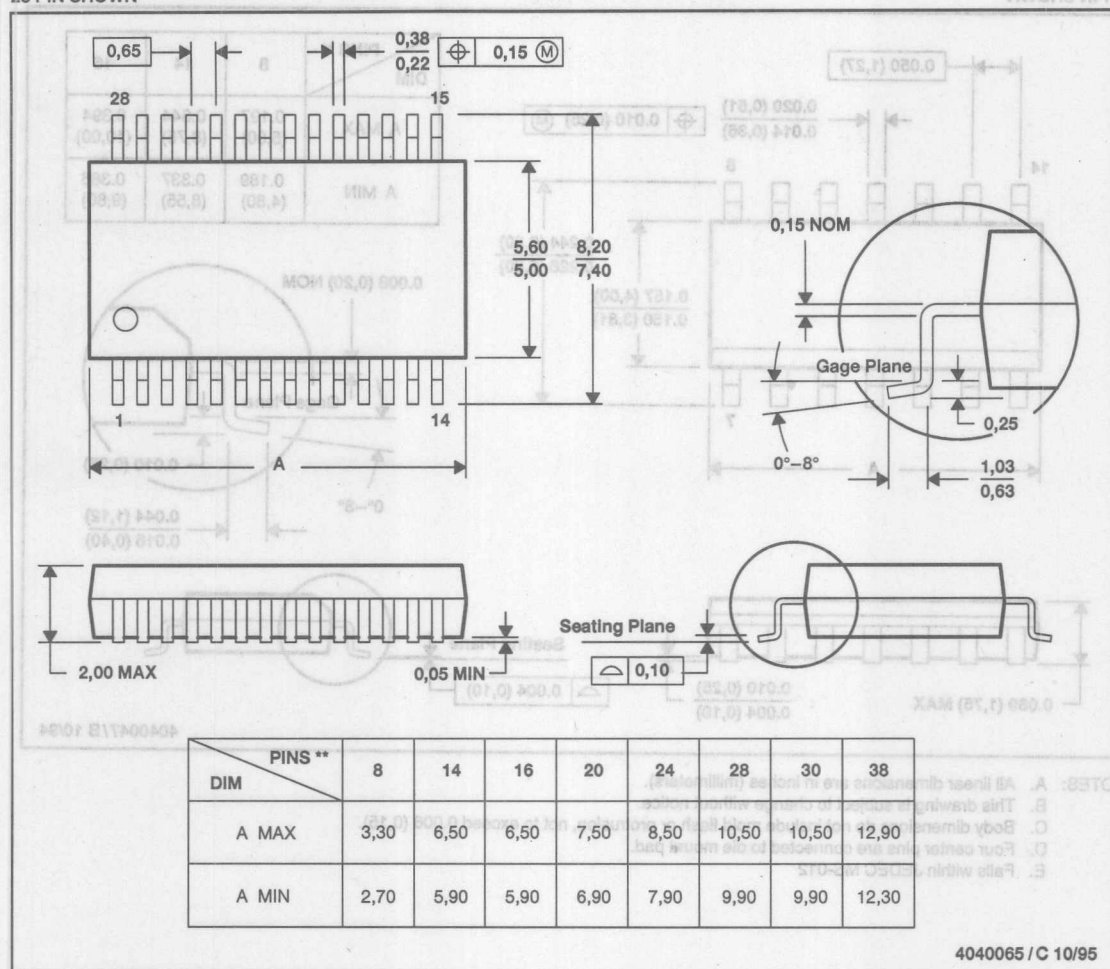
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
  - Four center pins are connected to die mount pad.
  - Falls within JEDEC MS-012

# MECHANICAL DATA

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

28 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150



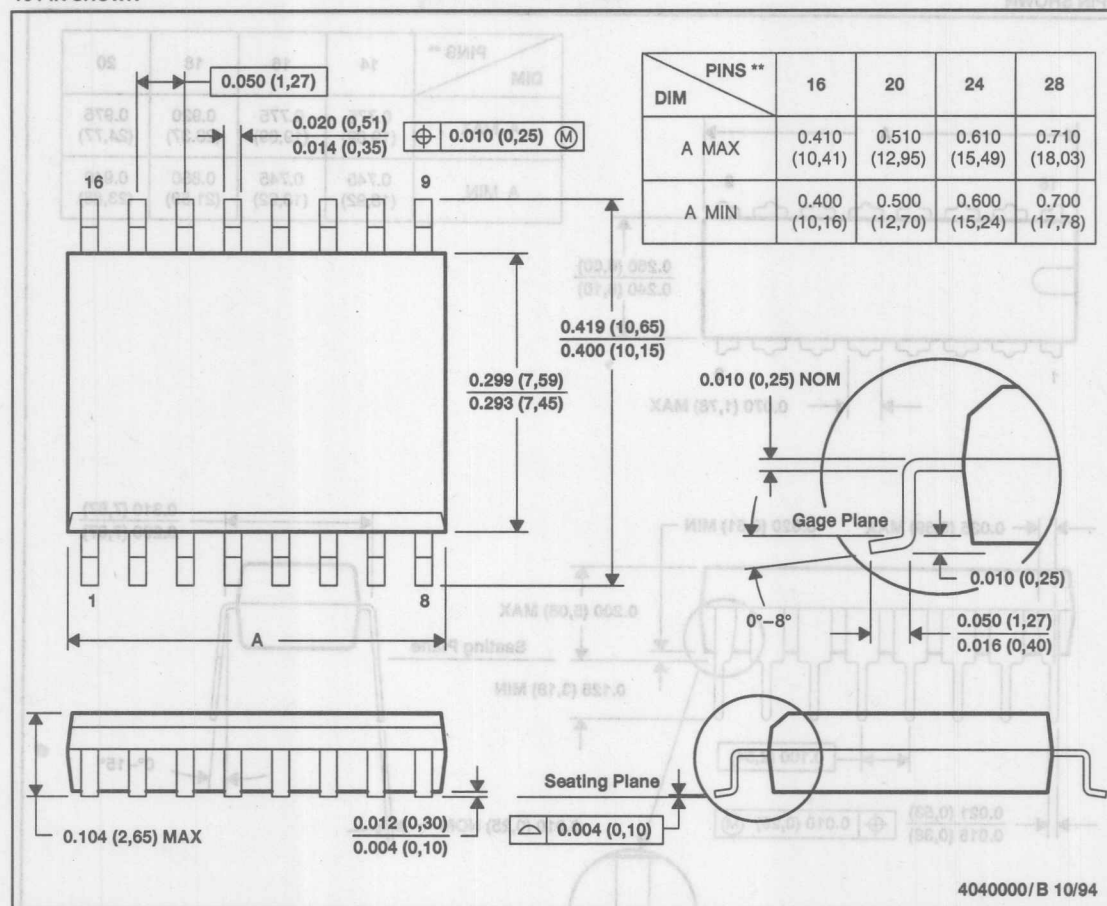
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# MECHANICAL DATA

DW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013



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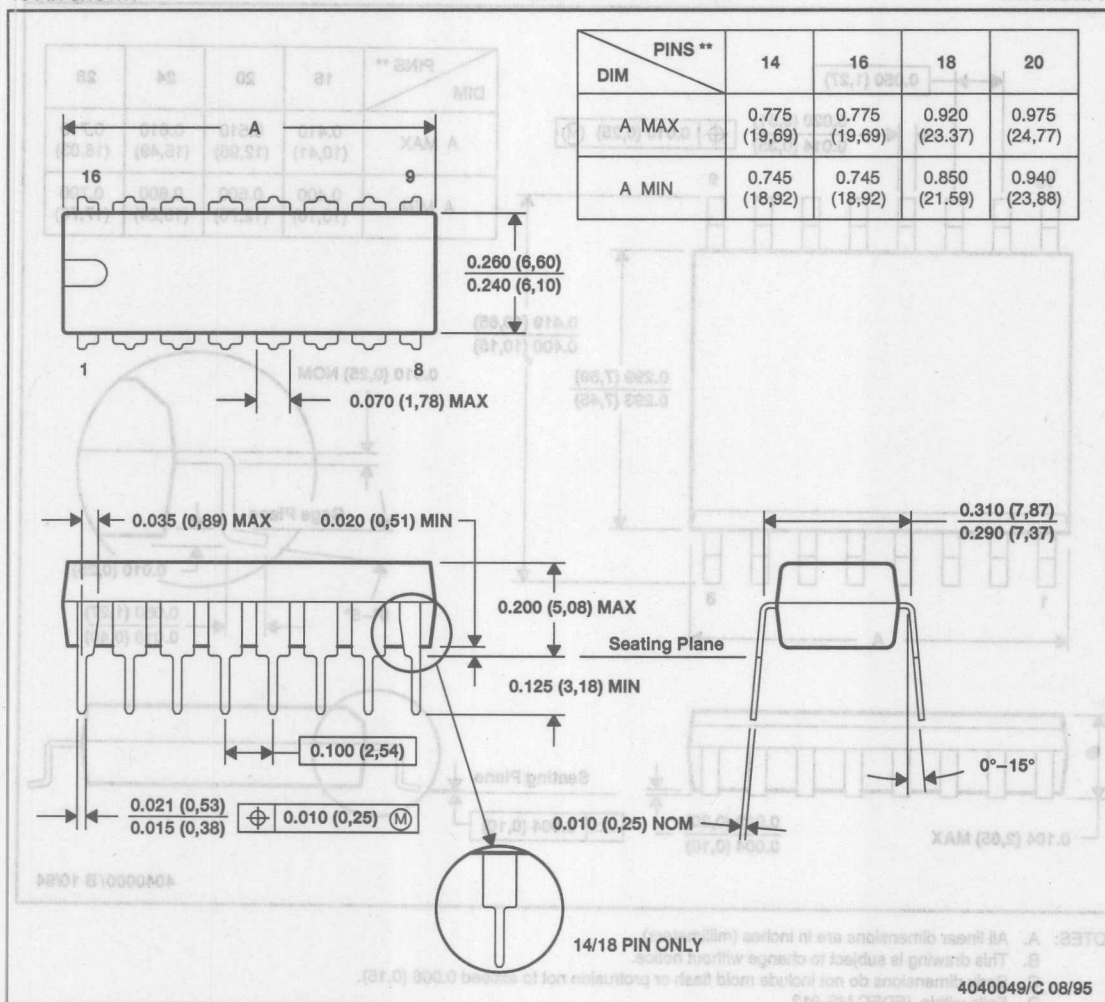
# MECHANICAL DATA

N (R-PDIP-T\*\*)

16 PIN SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

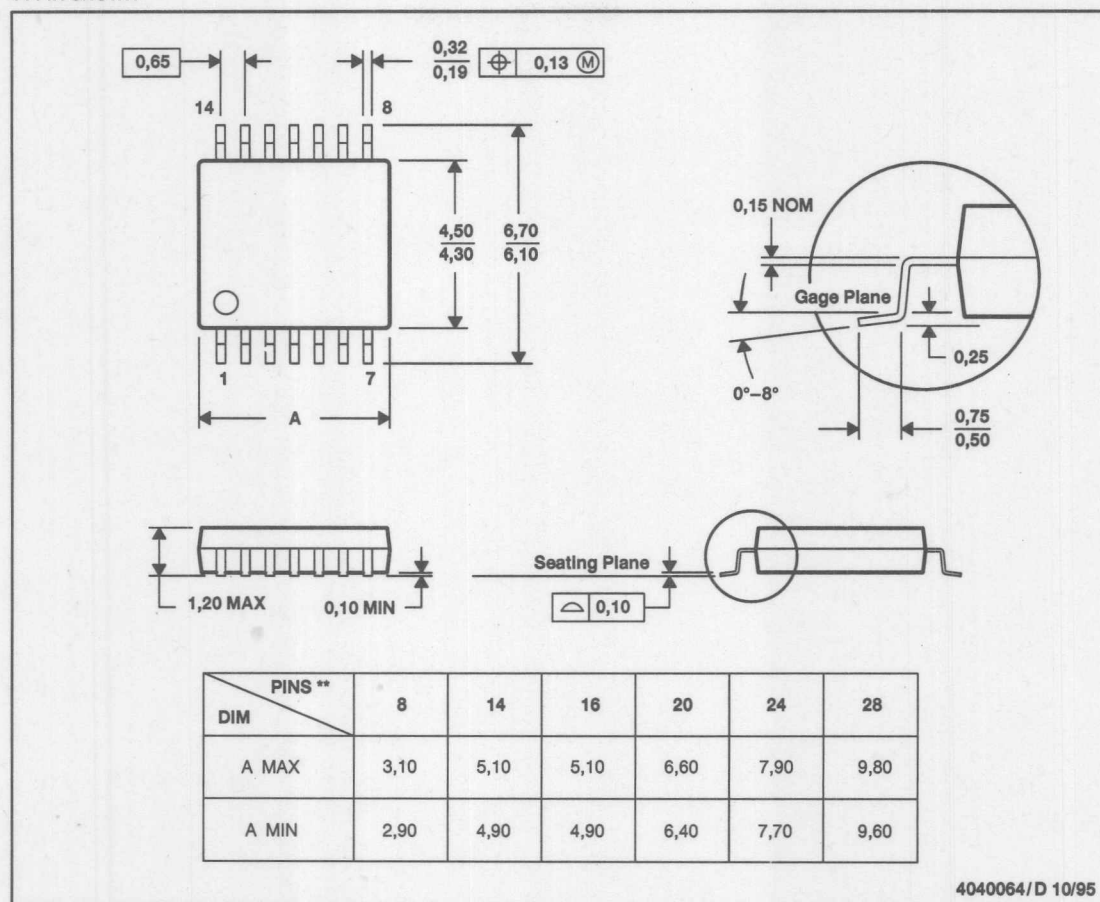


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PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



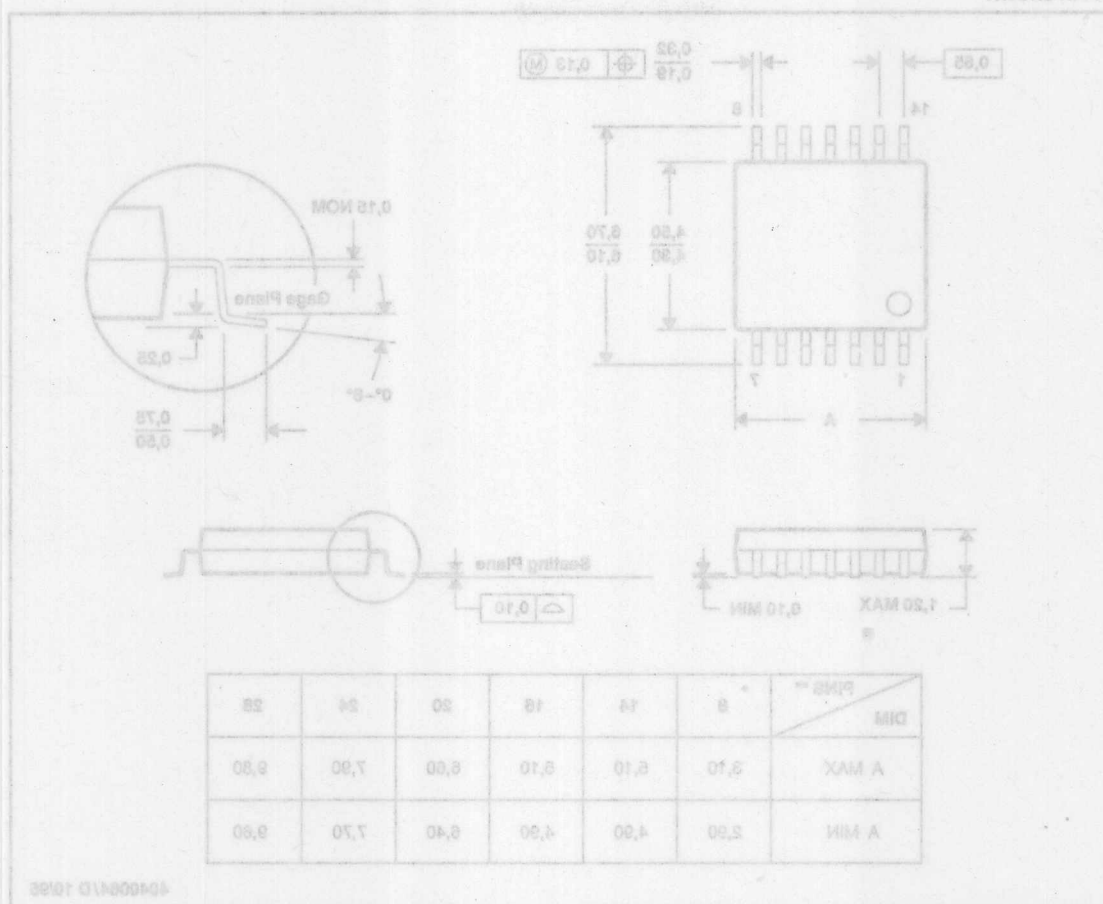
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



PLASTIC SMALL-OUTLINE PACKAGE

PW (R-PDSO-G\*\*)

14 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.18.  
 D. Falls within JEDEC MO-100.

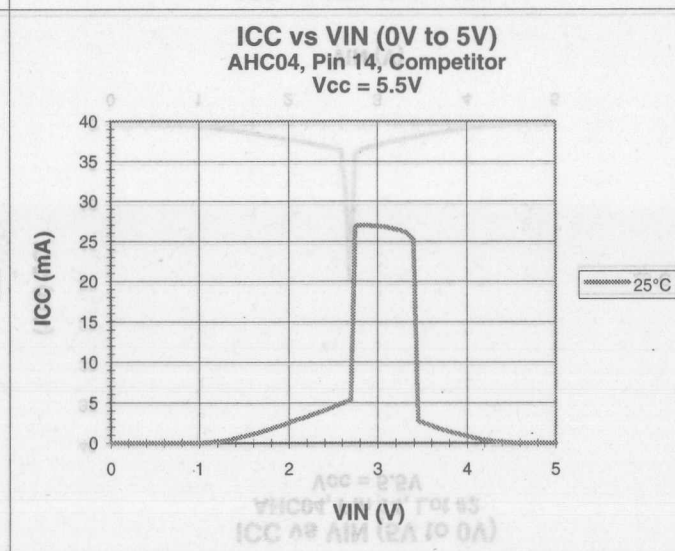
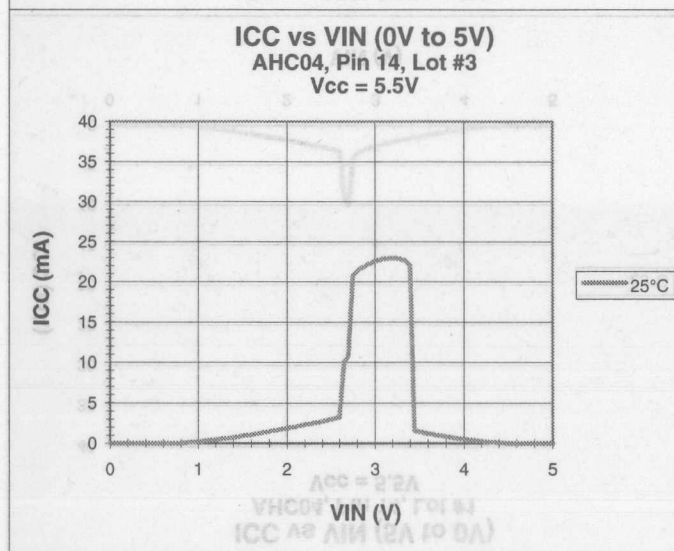
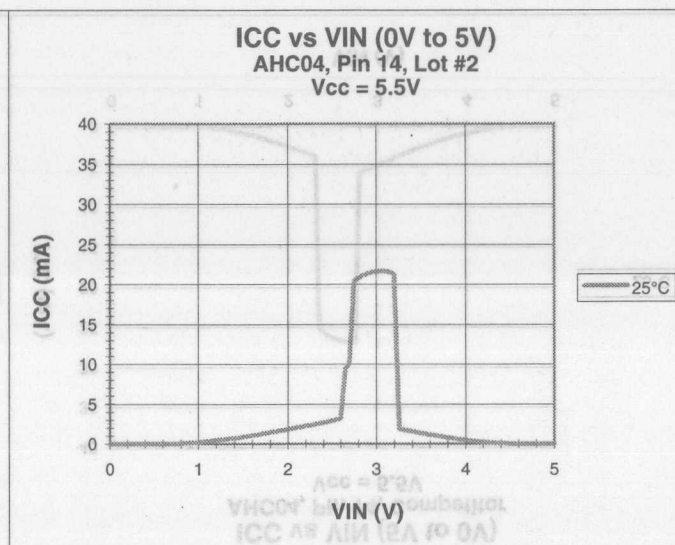
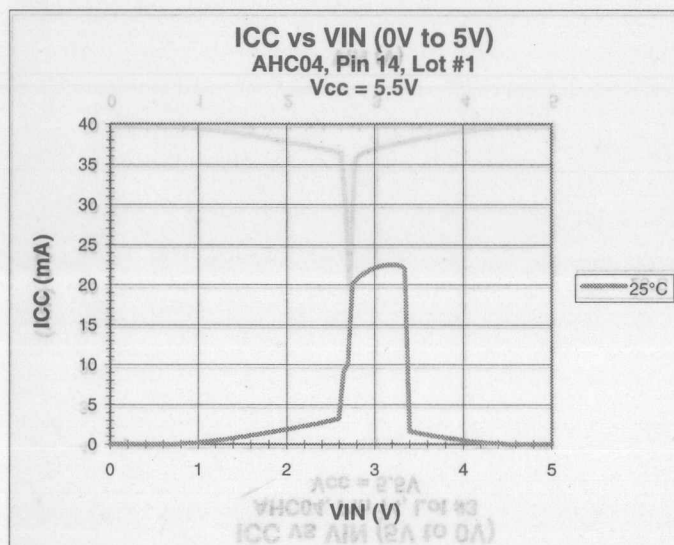
<b>General Information</b>	<b>1</b>
<b>AHC Data Sheets</b>	<b>2</b>
<b>AHCT Data Sheets</b>	<b>3</b>
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<b>AHC245 Qualification Data</b>	<b>C</b>
<b>AHCT245 Qualification Data</b>	<b>D</b>

Qualification Data

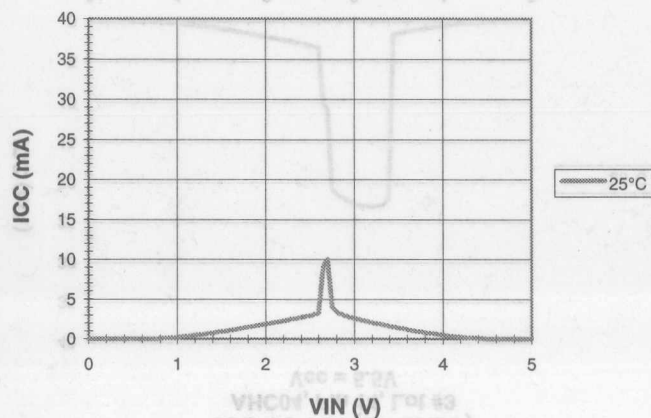
1	General Information
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4	Technical Data

A	AHC04 Qualification Data
	AHCT04 Qualification Data
	AHCT05 Qualification Data
	AHCT06 Qualification Data

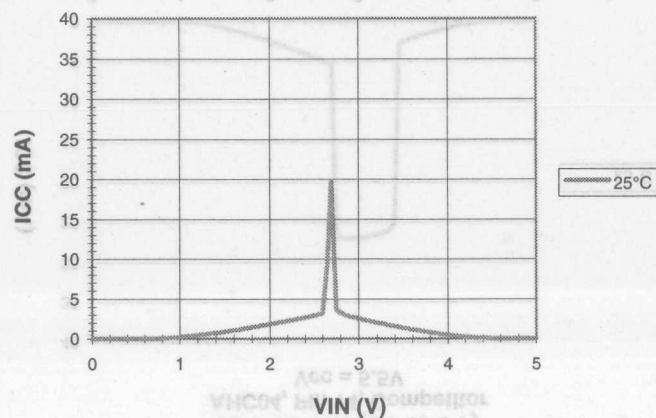
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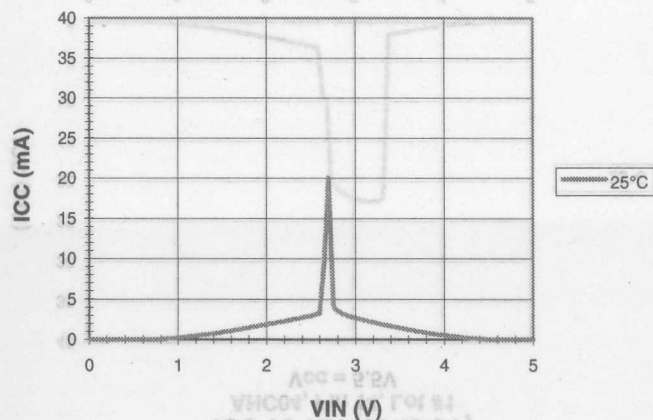
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AHC04, Pin 14, Lot #1  
Vcc = 5.5V



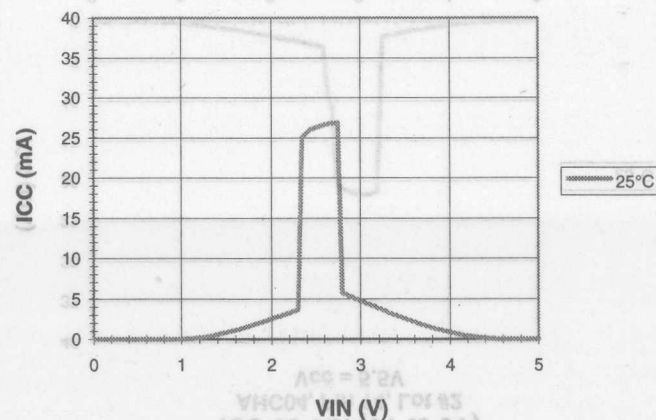
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Vcc = 5.5V



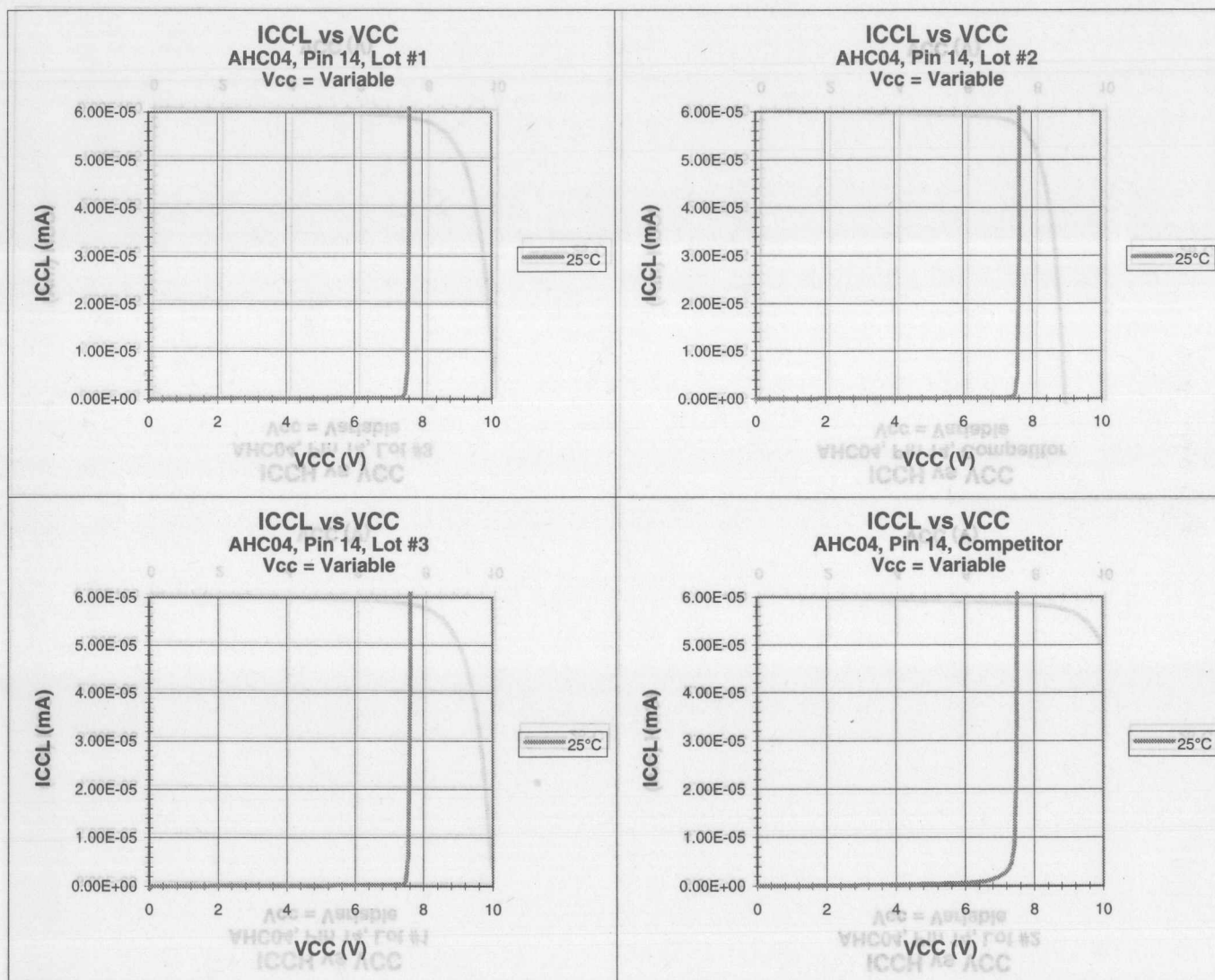
ICC vs VIN (5V to 0V)  
AHC04, Pin 14, Lot #3  
Vcc = 5.5V

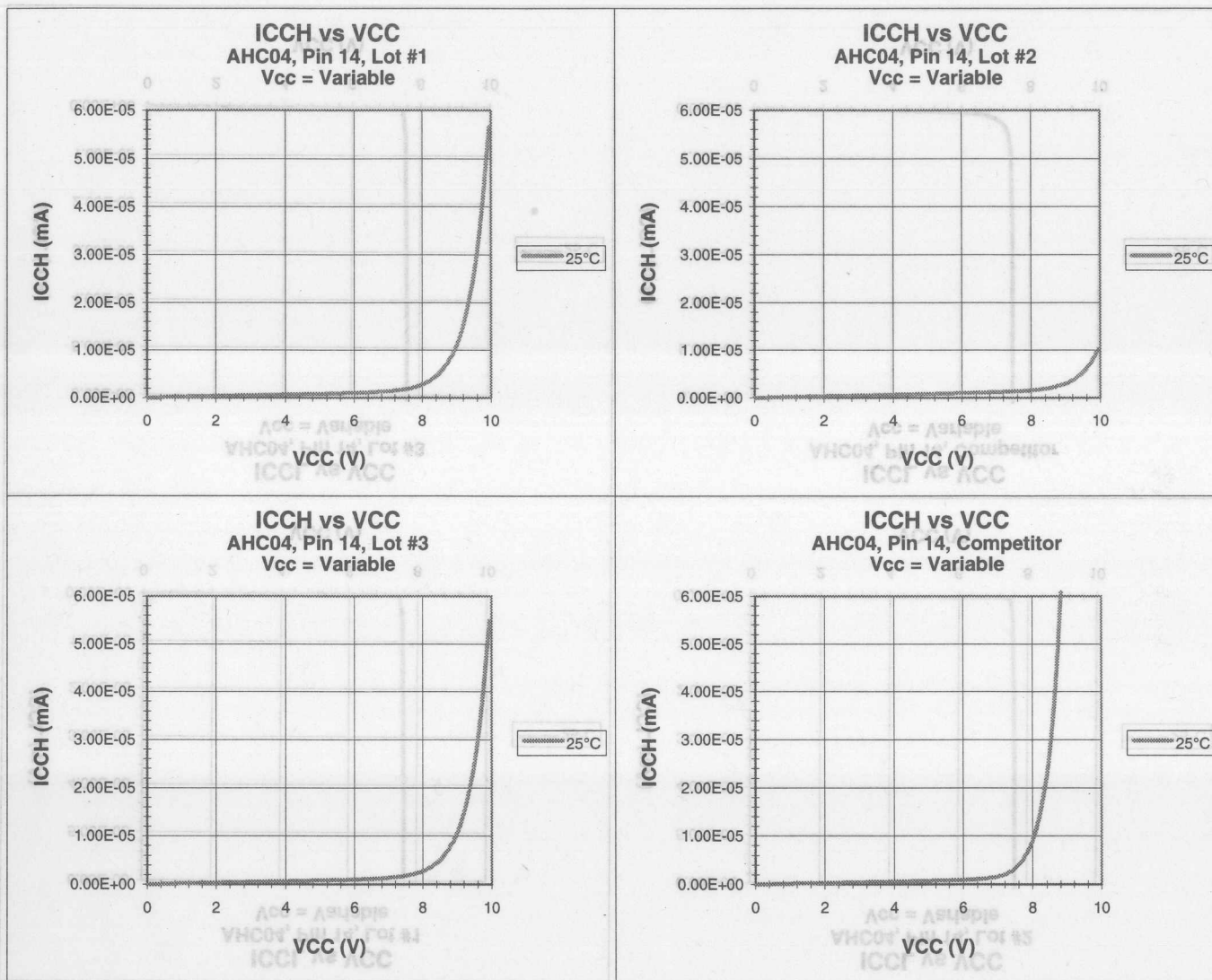


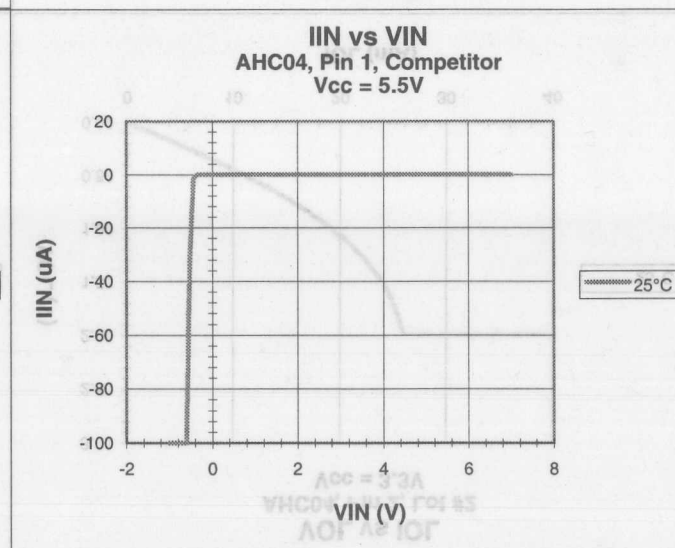
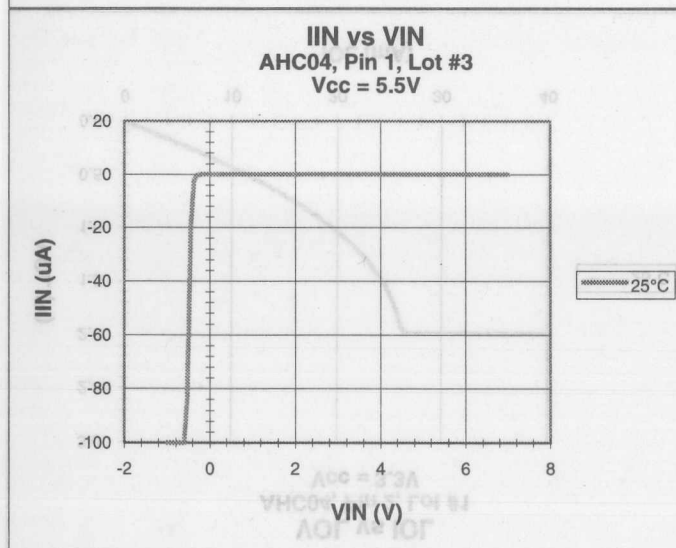
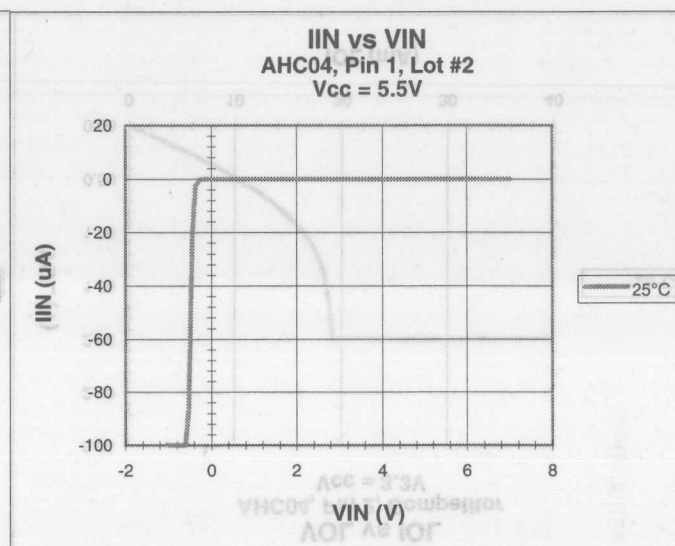
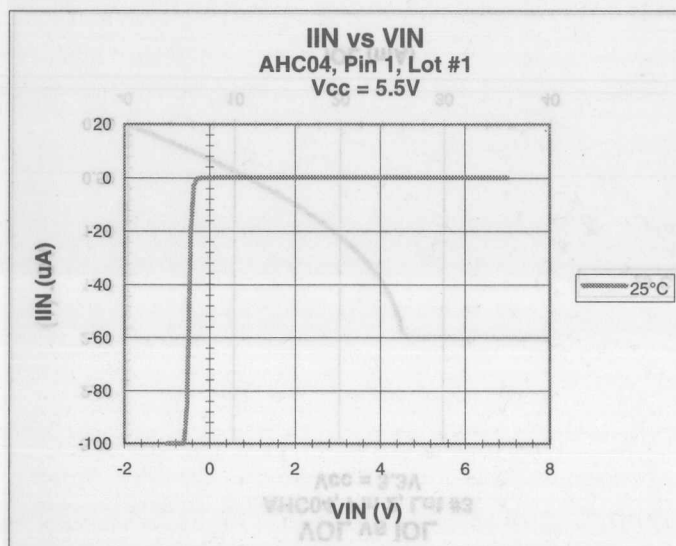
ICC vs VIN (5V to 0V)  
AHC04, Pin 14, Competitor  
Vcc = 5.5V



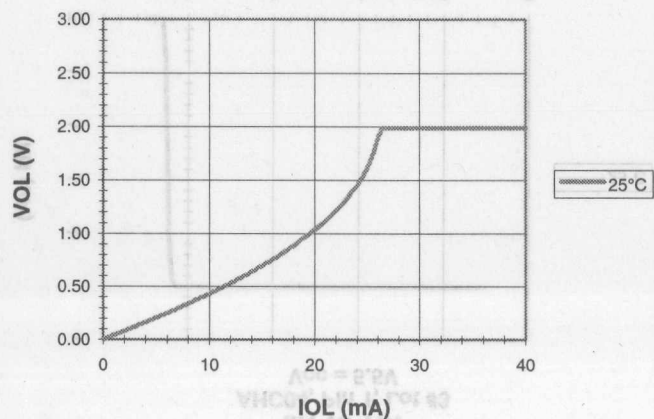




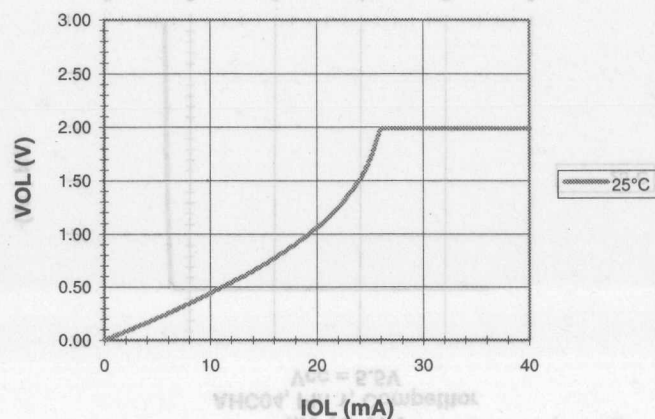




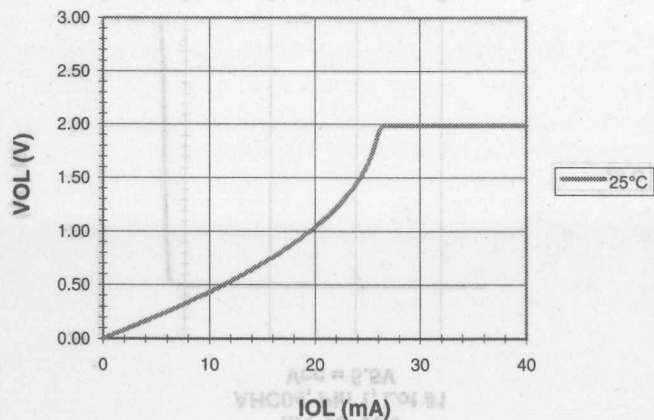
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Vcc = 3.3V



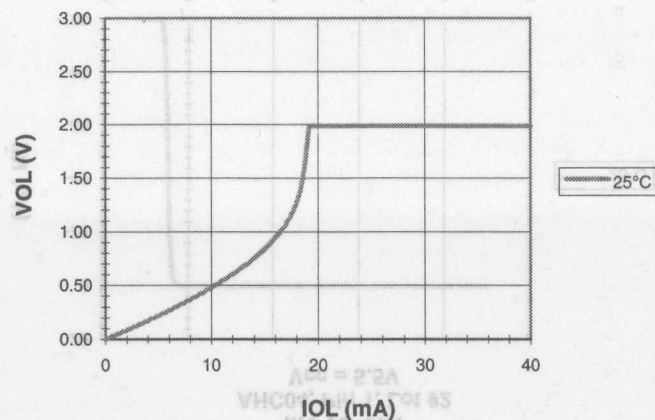
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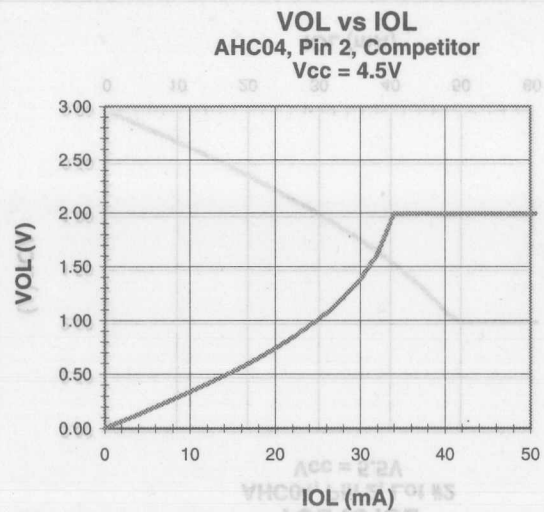
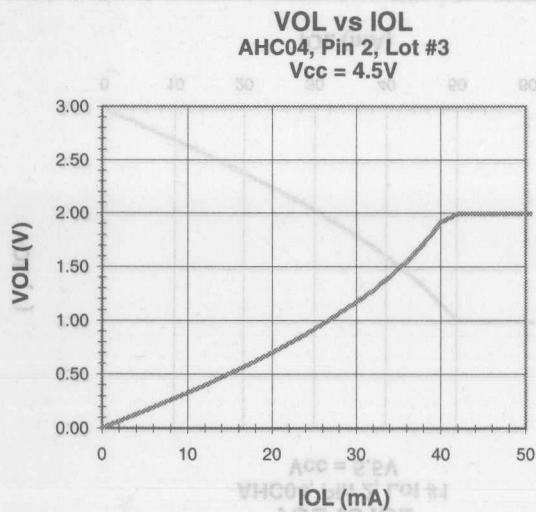
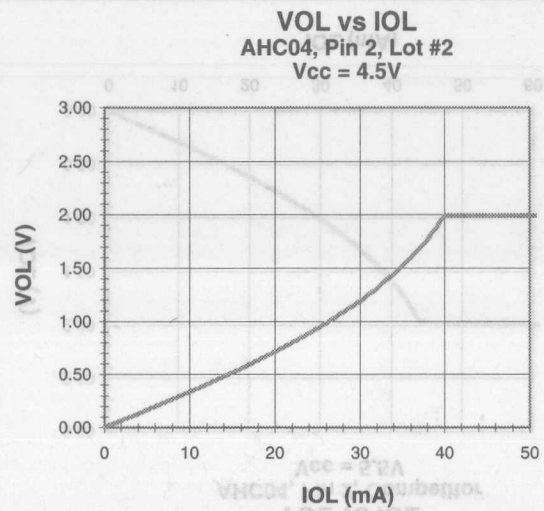
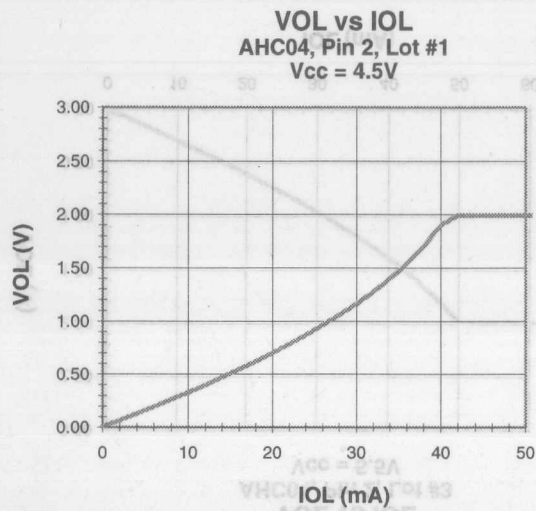


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AHC04, Pin 2, Lot #3  
Vcc = 3.3V



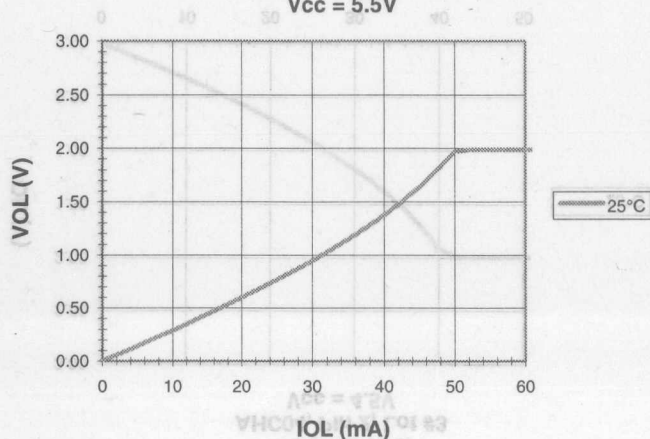
**VOL vs IOL**  
AHC04, Pin 2, Competitor  
Vcc = 3.3V



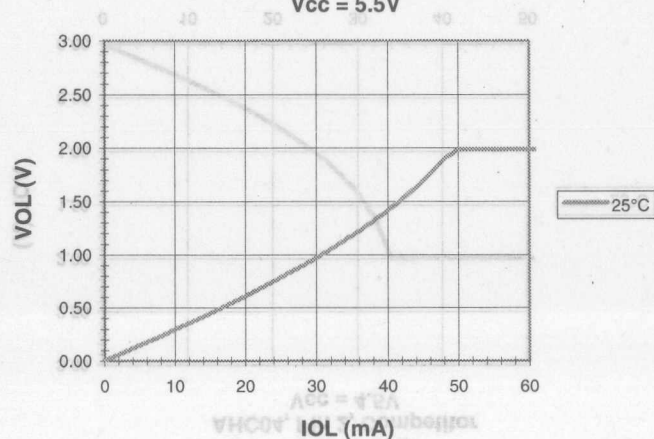




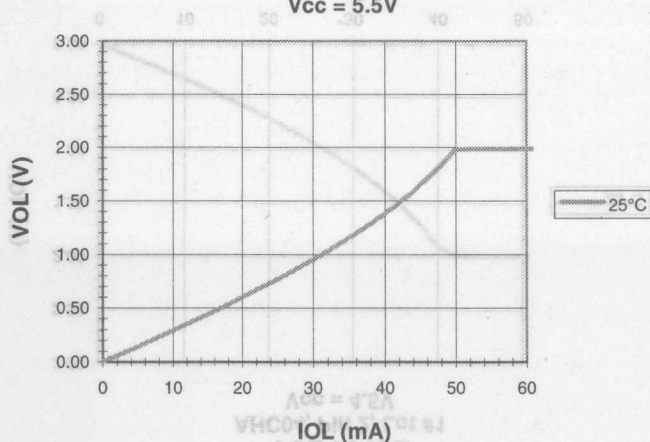
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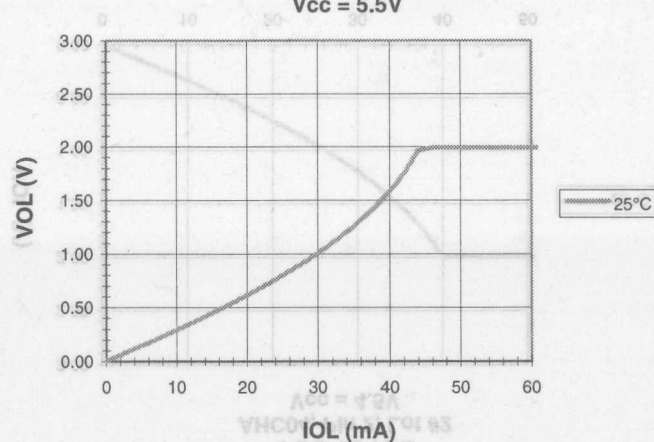
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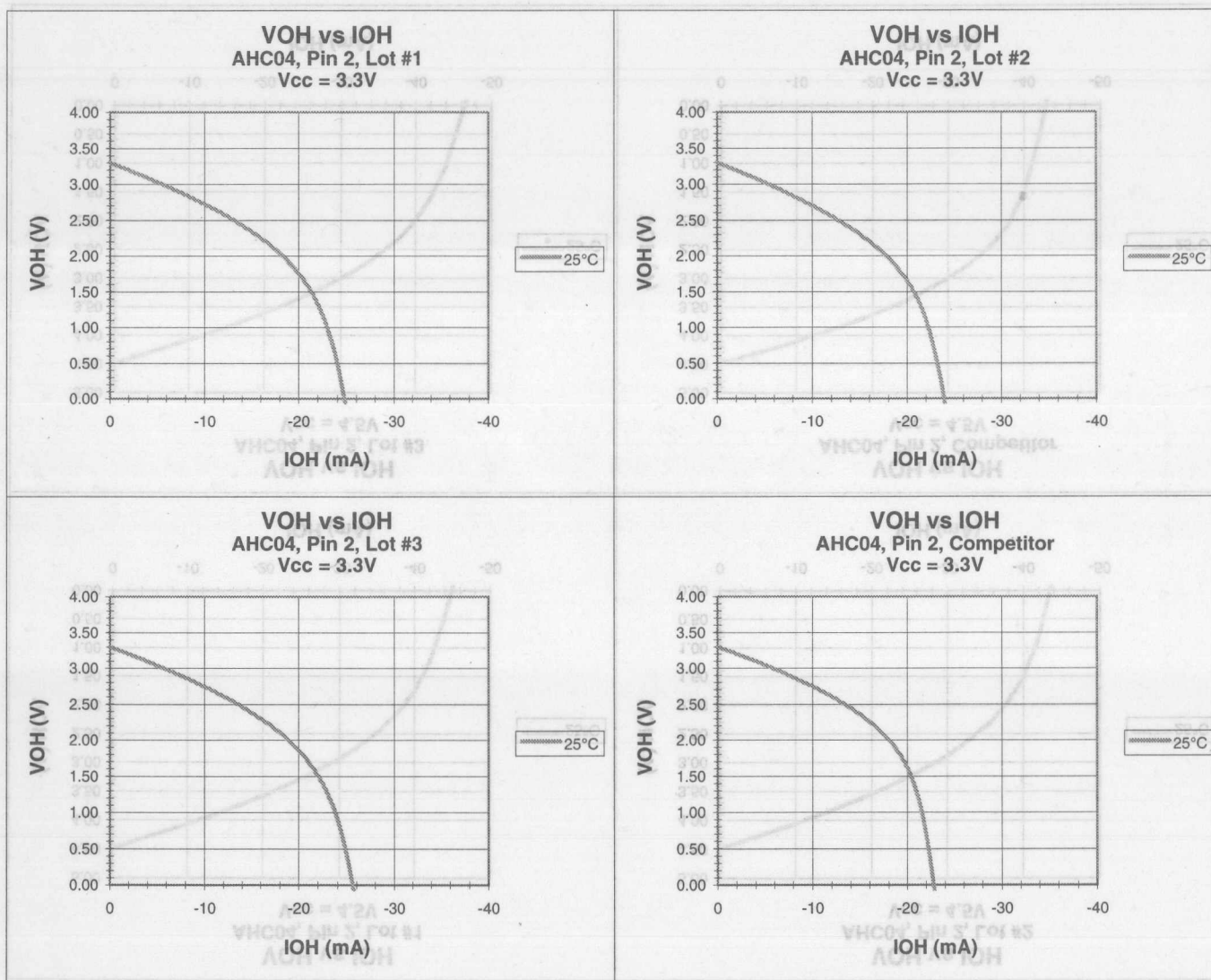


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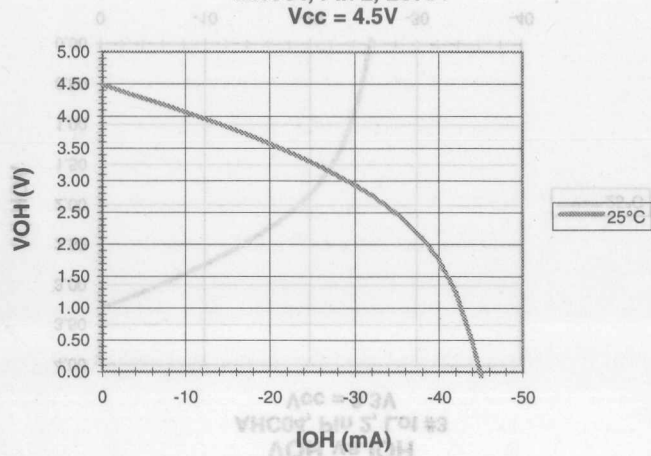


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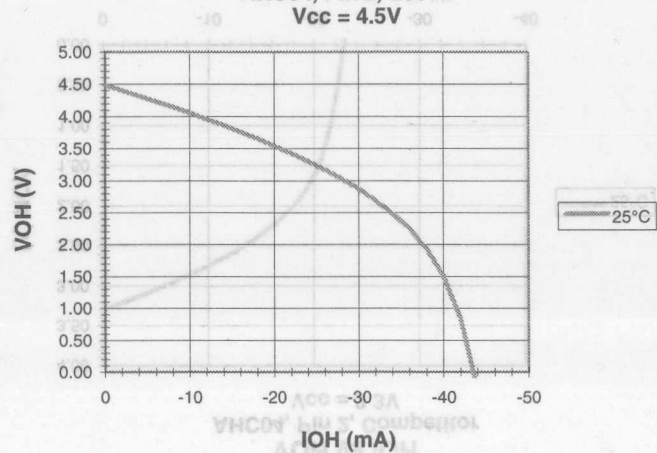




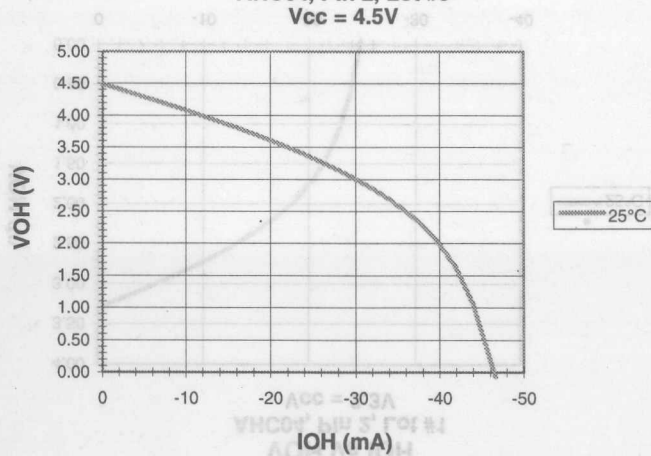
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AHC04, Pin 2, Lot #1  
Vcc = 4.5V



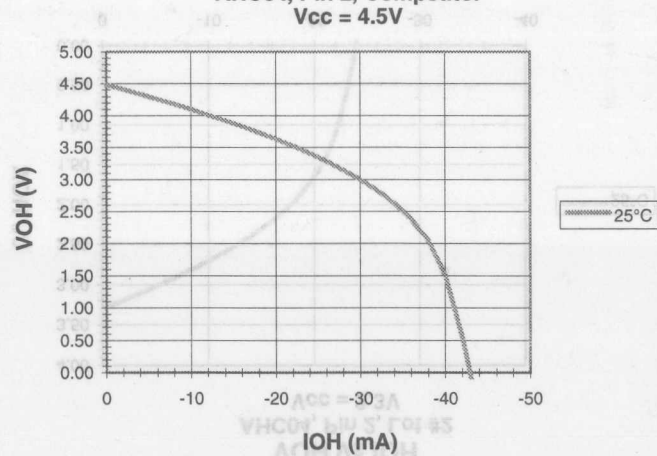
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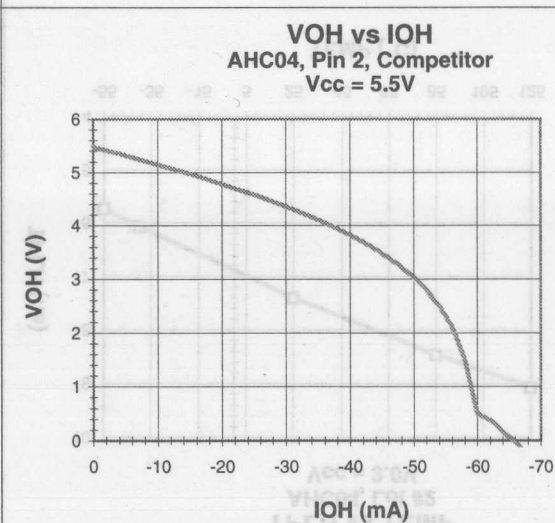
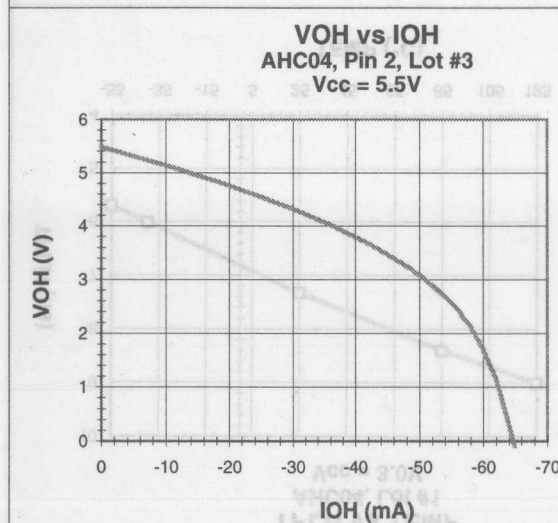
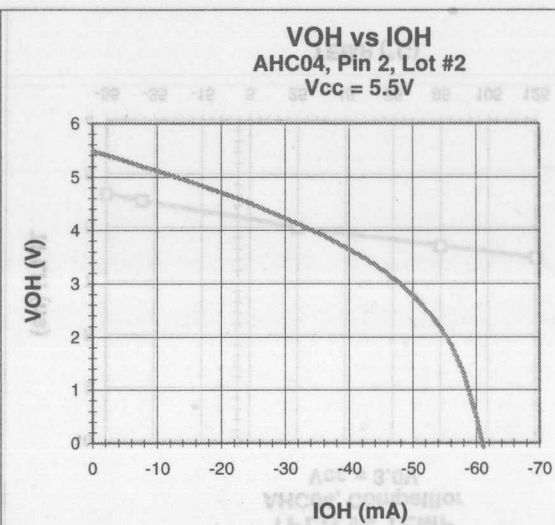
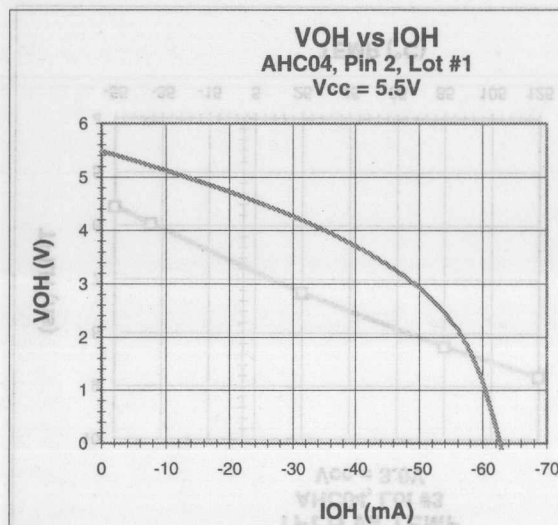


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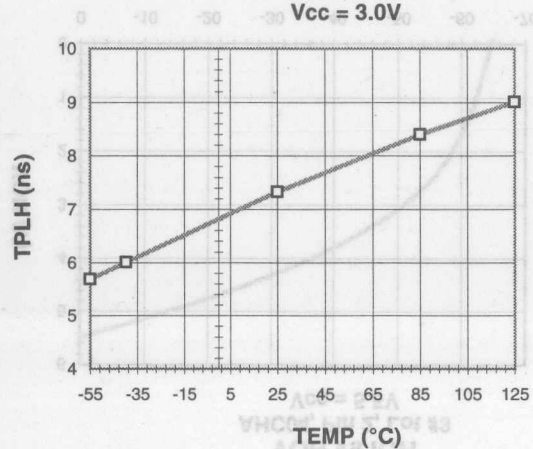


**VOH vs IOH**  
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Vcc = 4.5V

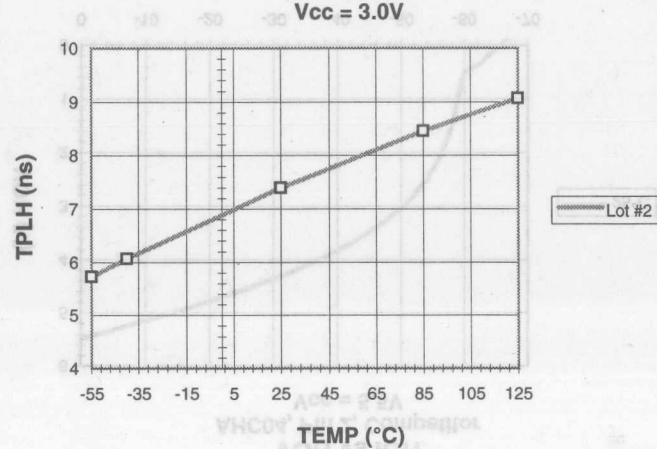




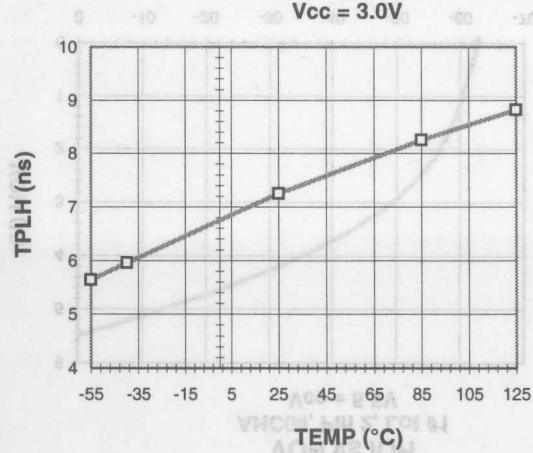
**TPLH vs TEMP**  
AHC04, Lot #1  
Vcc = 3.0V



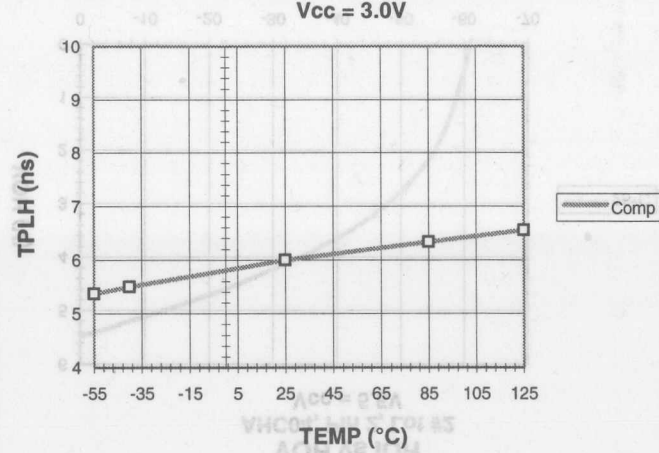
**TPLH vs TEMP**  
AHC04, Lot #2  
Vcc = 3.0V



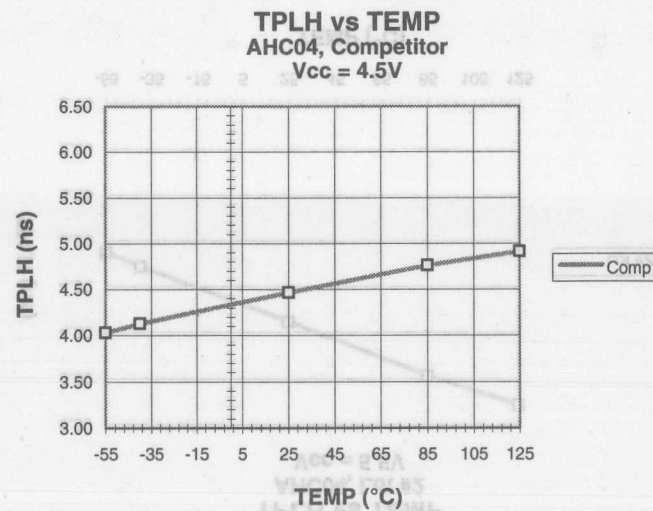
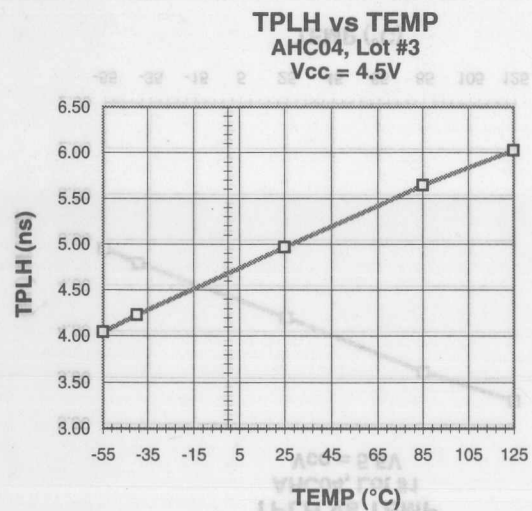
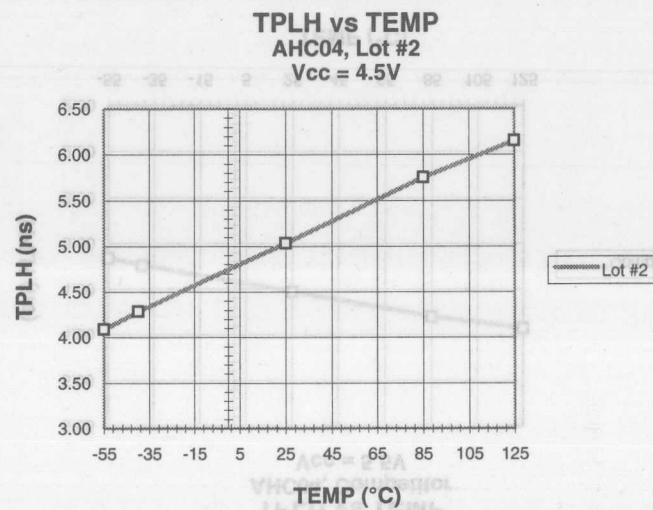
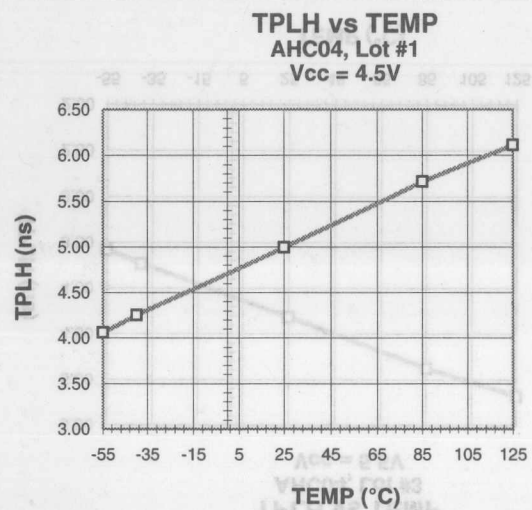
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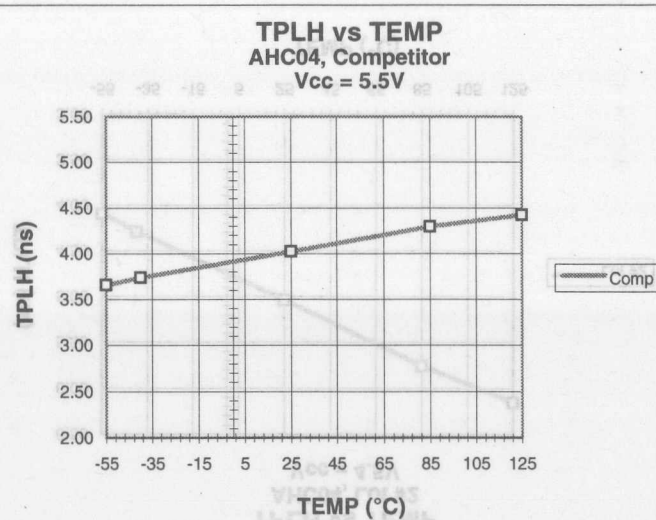
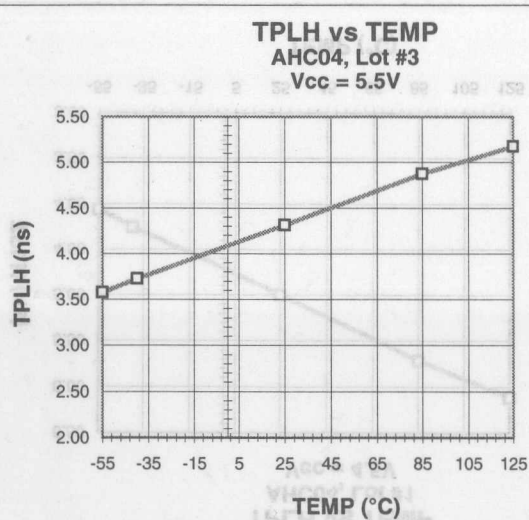
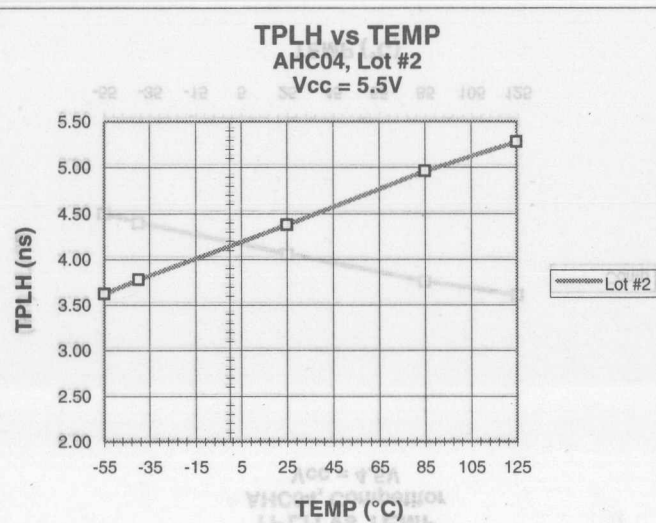
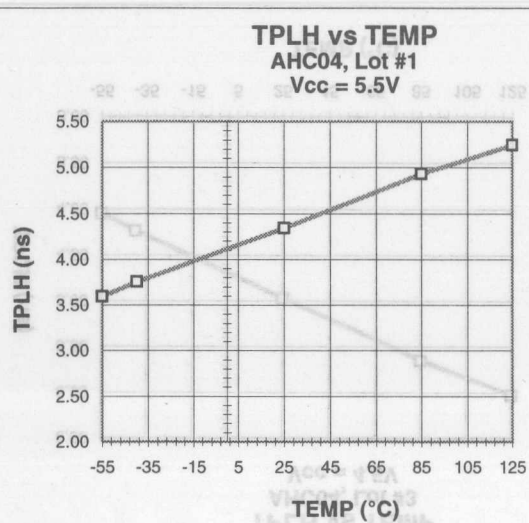


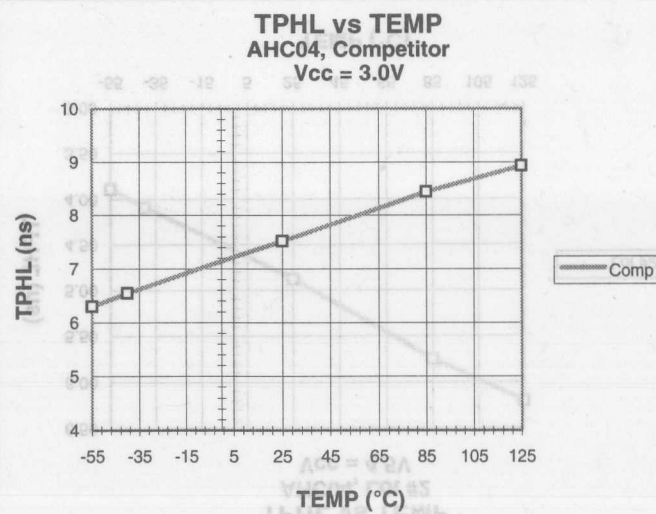
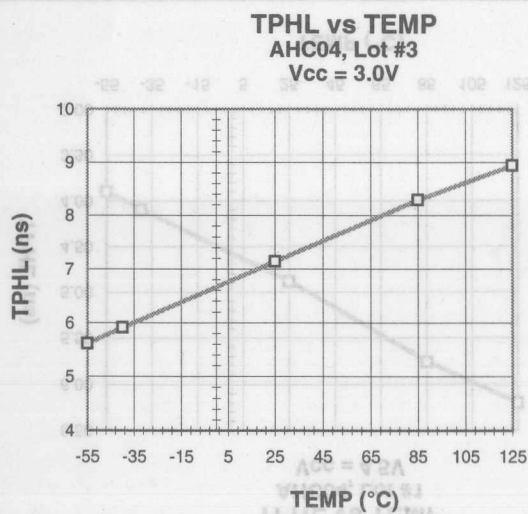
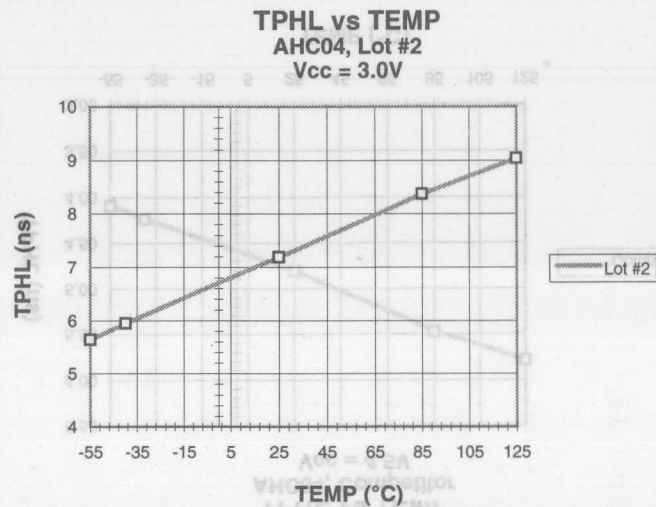
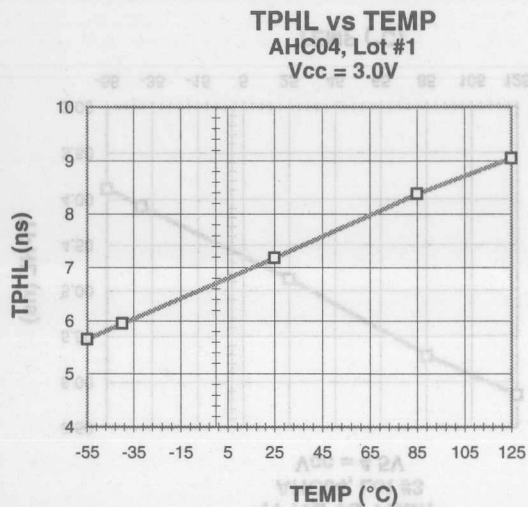
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AHC04, Competitor  
Vcc = 3.0V



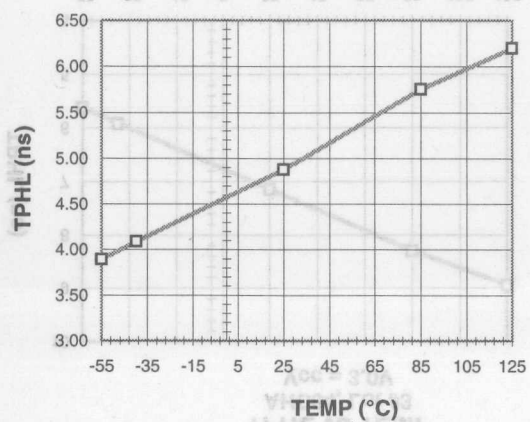




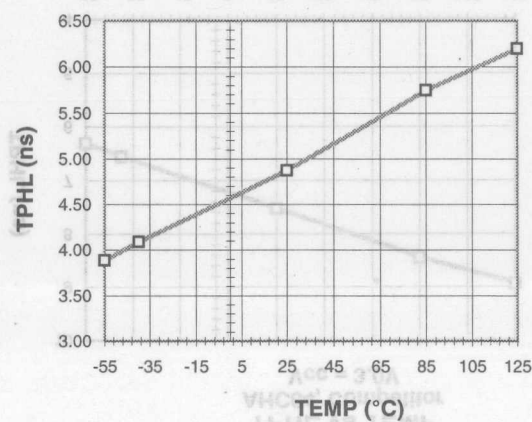




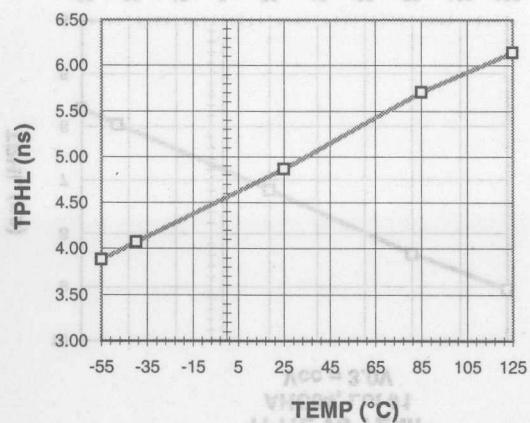
**TPHL vs TEMP**  
AHC04, Lot #1  
Vcc = 4.5V



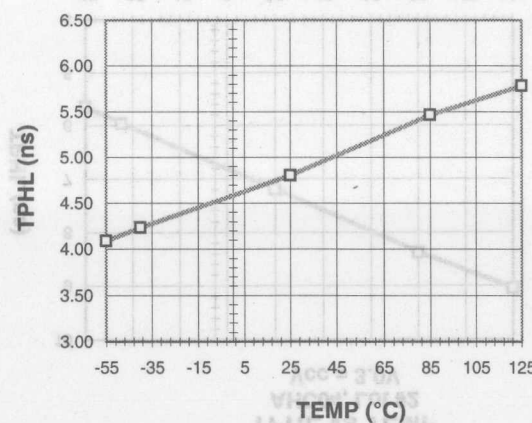
**TPHL vs TEMP**  
AHC04, Lot #2  
Vcc = 4.5V

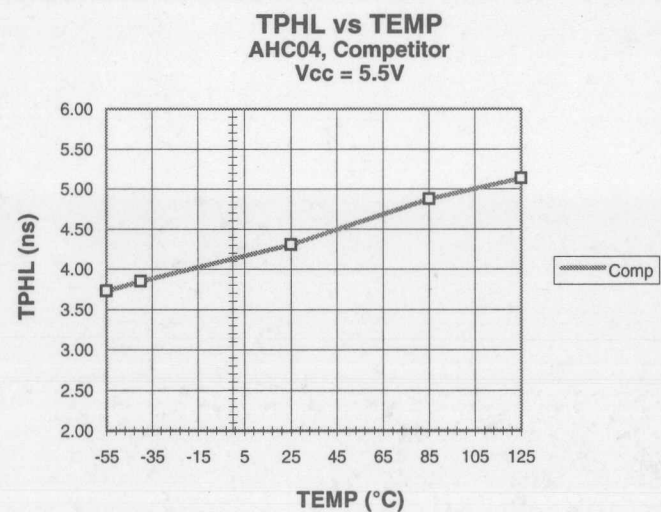
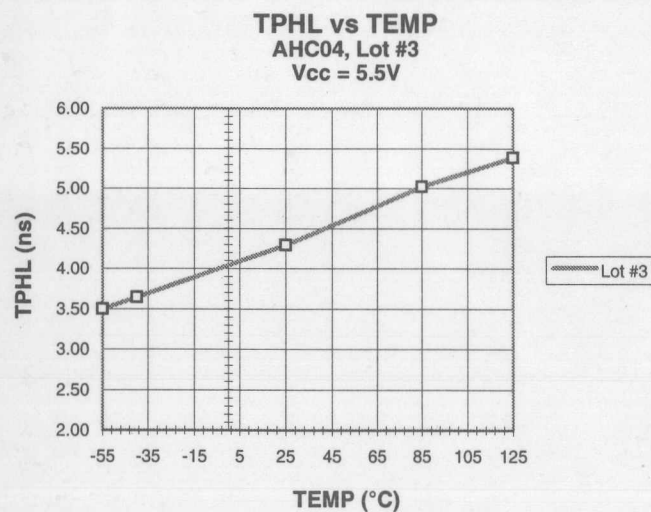
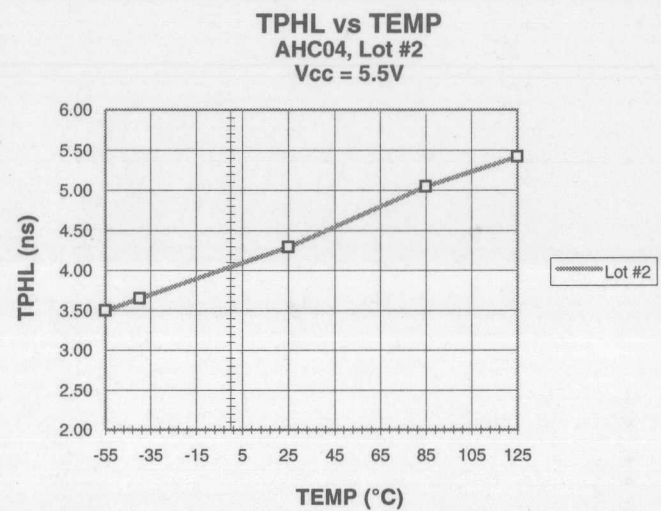
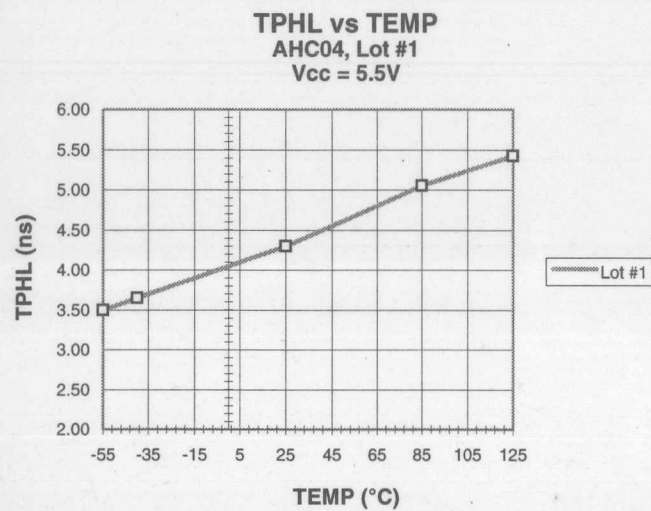


**TPHL vs TEMP**  
AHC04, Lot #3  
Vcc = 4.5V



**TPHL vs TEMP**  
AHC04, Competitor  
Vcc = 4.5V









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Qualification Data

1

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A

AHCT04 Qualification Data

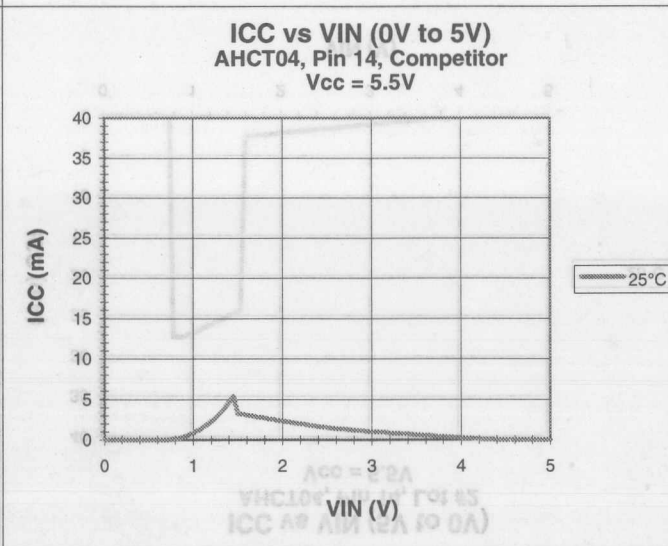
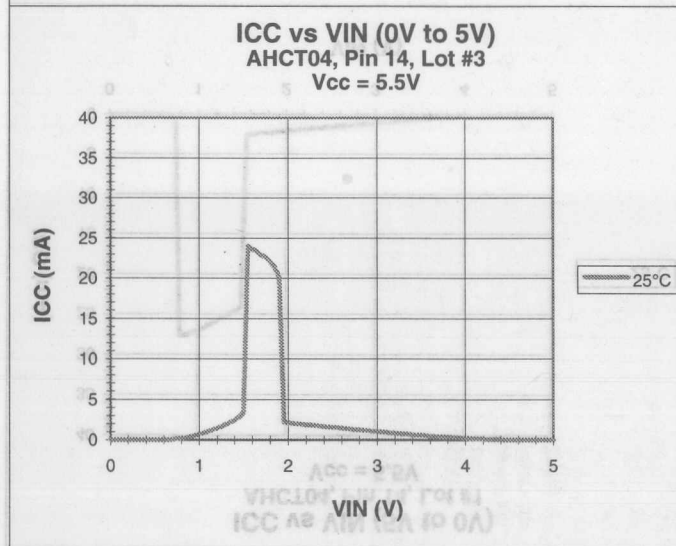
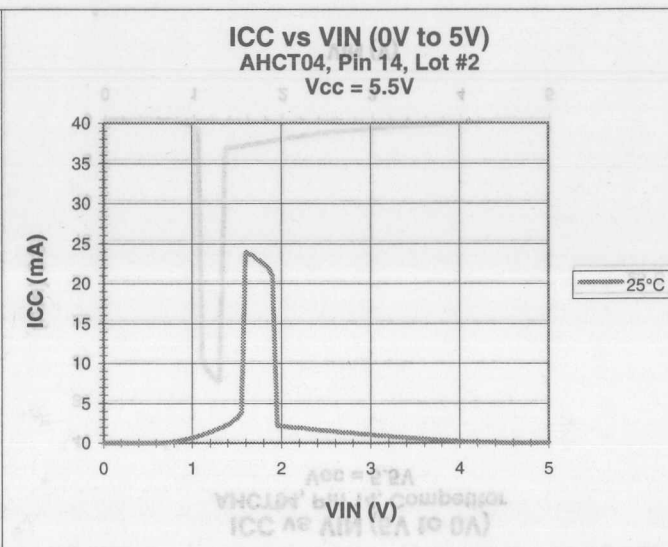
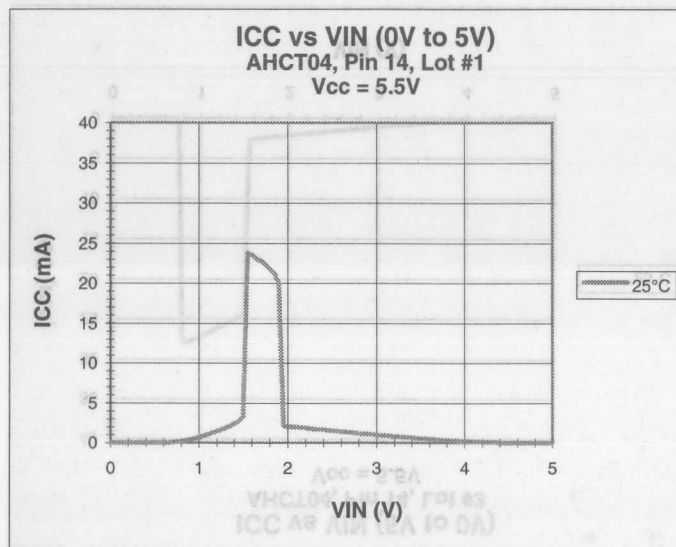
**B**

AHCT04 Qualification Data

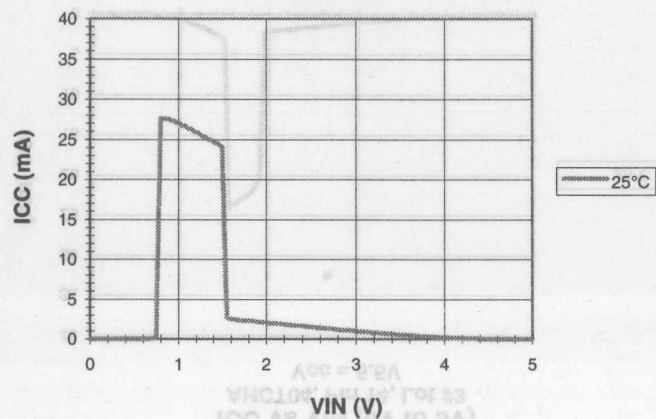
# AHCT04 Qualification Data

AHCT04 Qualification Data

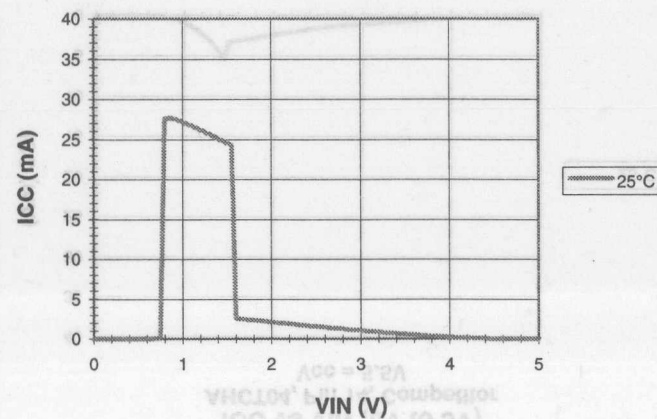
AHCT04 Qualification Data



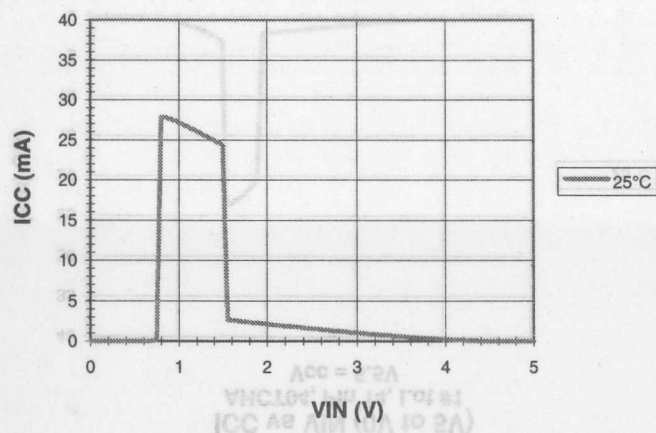
**ICC vs VIN (5V to 0V)**  
**AHCT04, Pin 14, Lot #1**  
**Vcc = 5.5V**



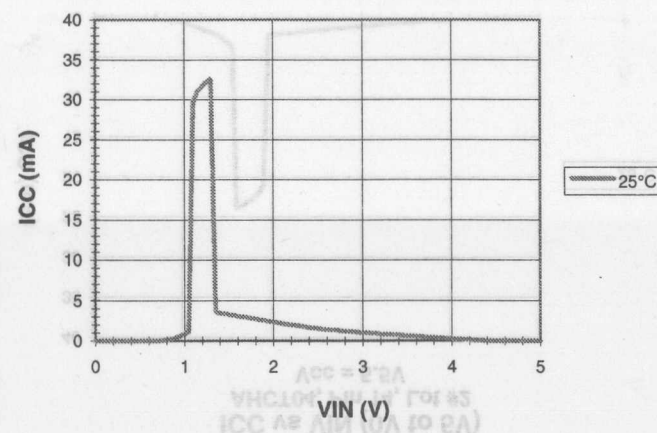
**ICC vs VIN (5V to 0V)**  
**AHCT04, Pin 14, Lot #2**  
**Vcc = 5.5V**



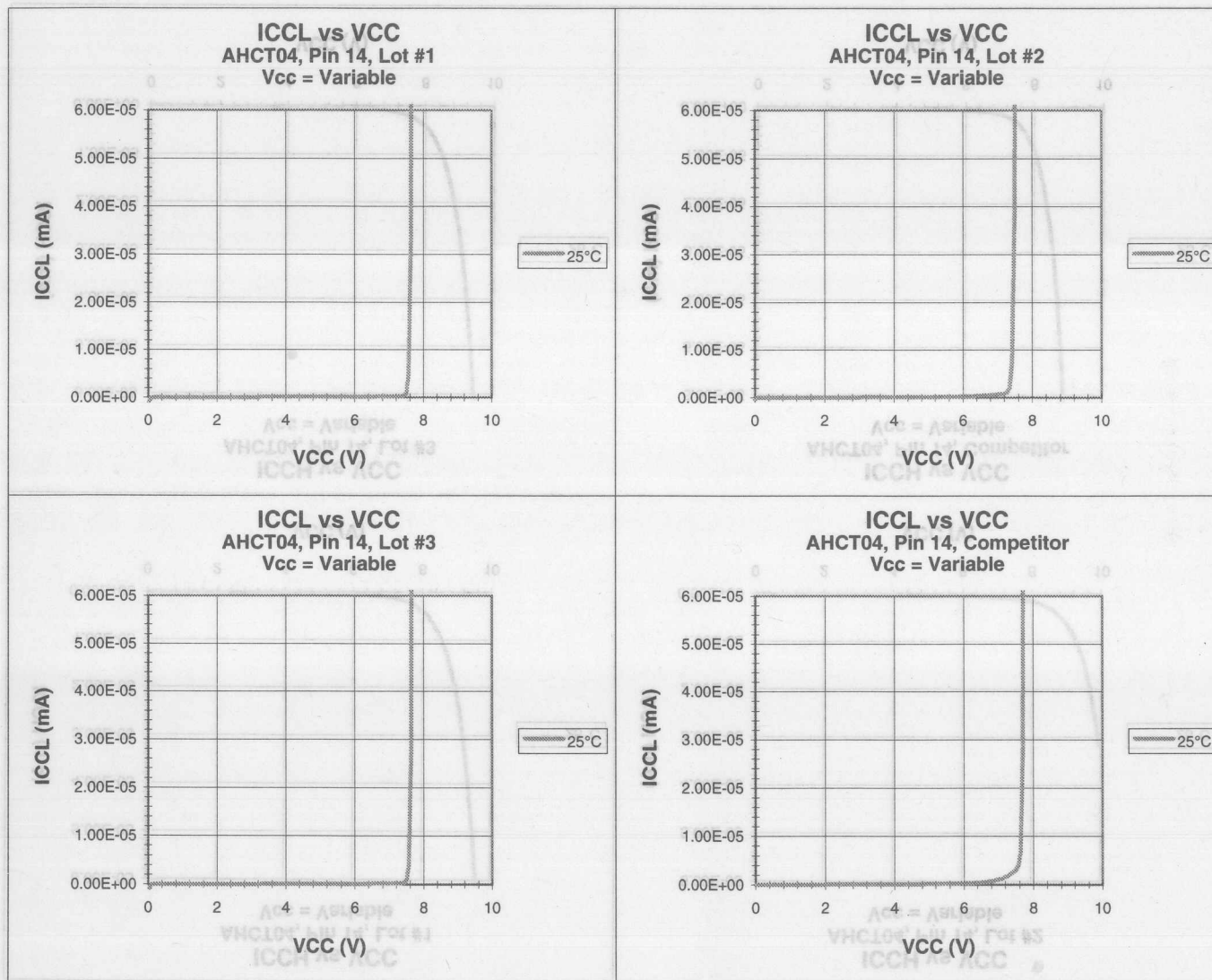
**ICC vs VIN (5V to 0V)**  
**AHCT04, Pin 14, Lot #3**  
**Vcc = 5.5V**



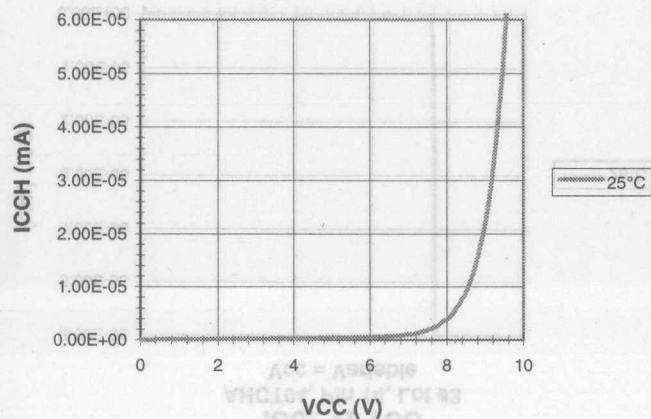
**ICC vs VIN (5V to 0V)**  
**AHCT04, Pin 14, Competitor**  
**Vcc = 5.5V**



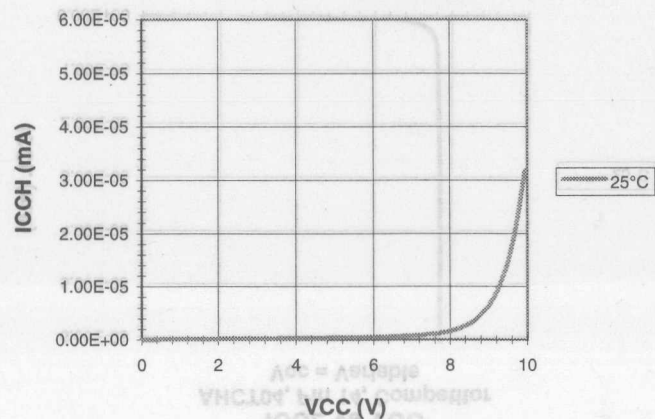




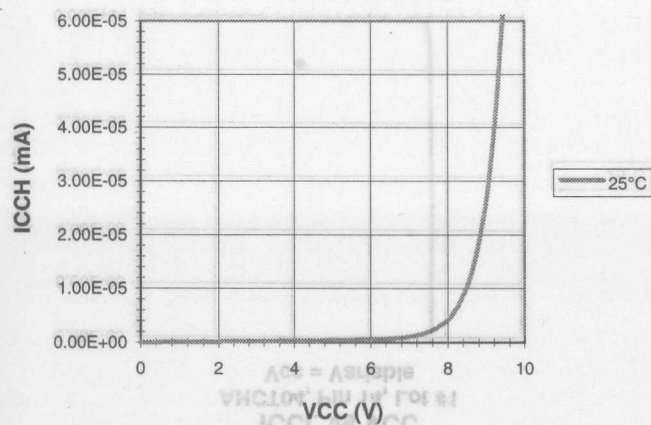
**ICCH vs VCC**  
AHCT04, Pin 14, Lot #1  
Vcc = Variable



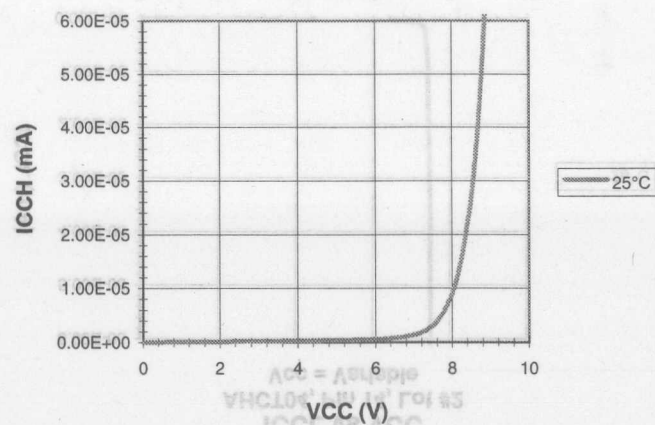
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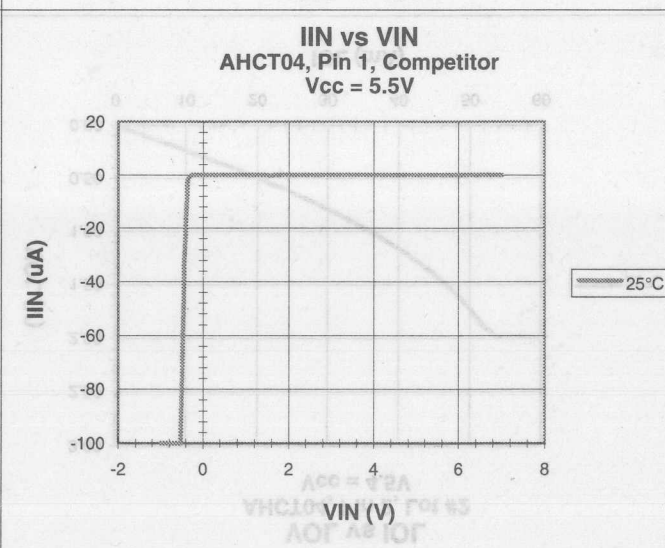
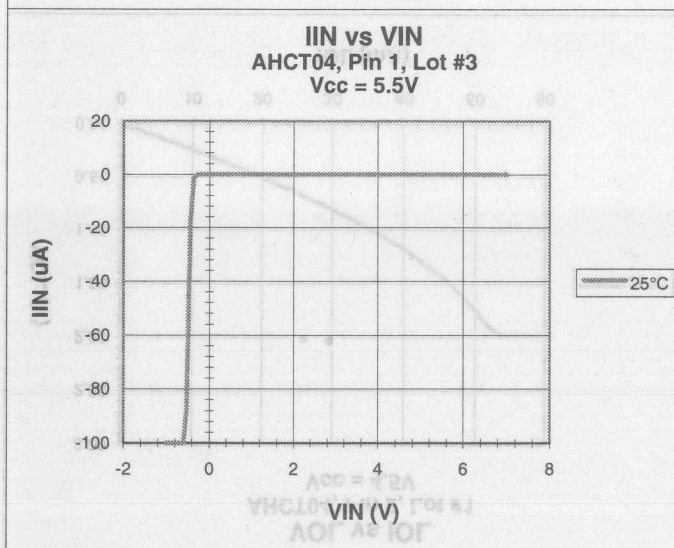
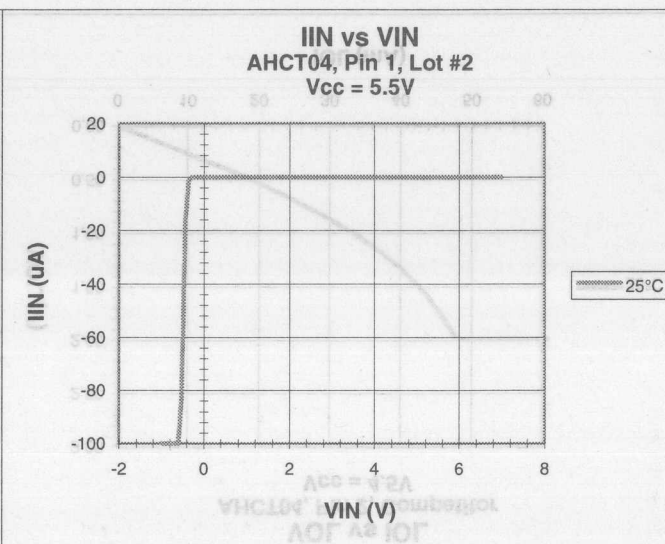
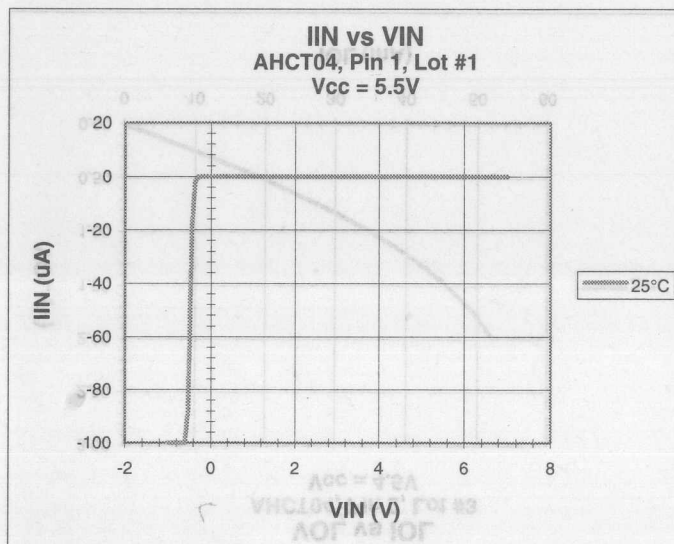


**ICCH vs VCC**  
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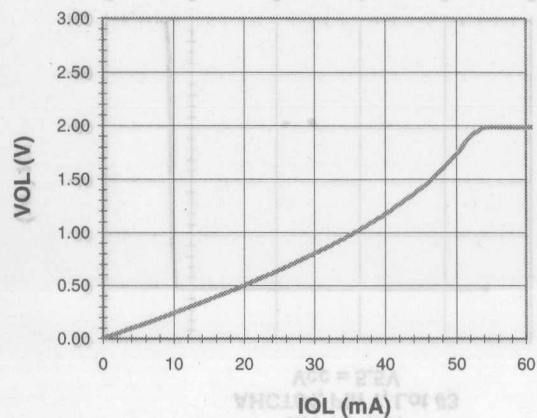


**ICCH vs VCC**  
AHCT04, Pin 14, Competitor  
Vcc = Variable

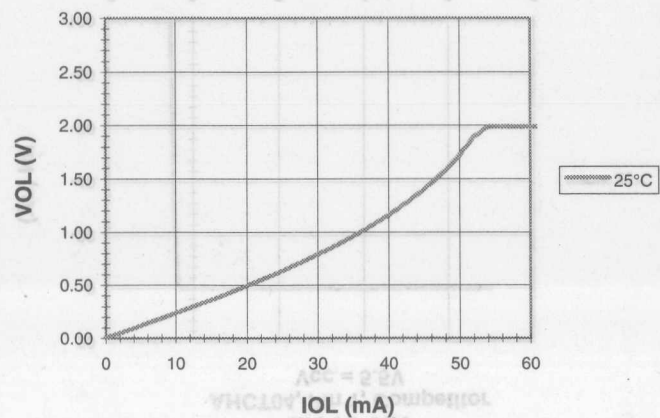




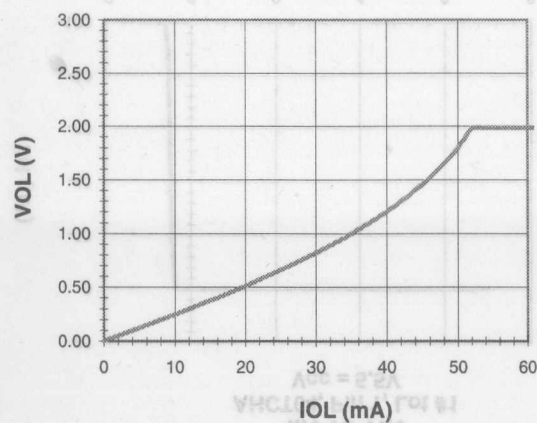
**VOL vs IOL**  
AHCT04, Pin 2, Lot #1  
Vcc = 4.5V



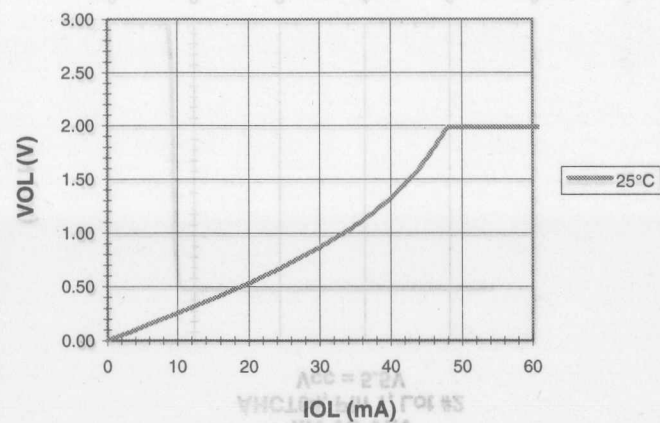
**VOL vs IOL**  
AHCT04, Pin 2, Lot #2  
Vcc = 4.5V

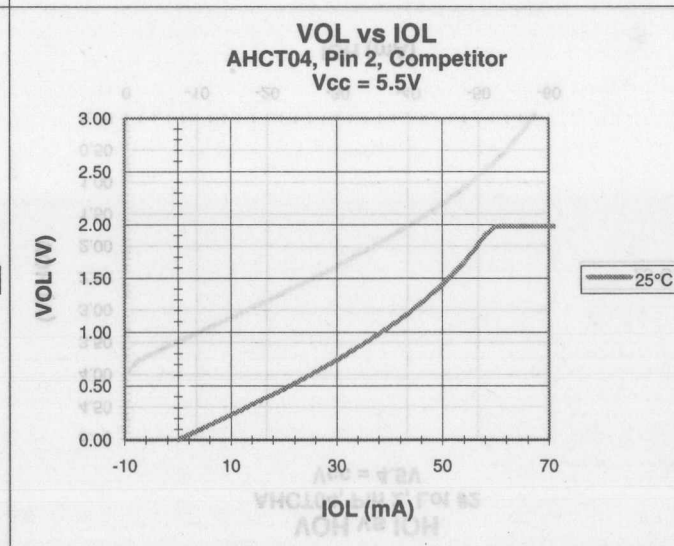
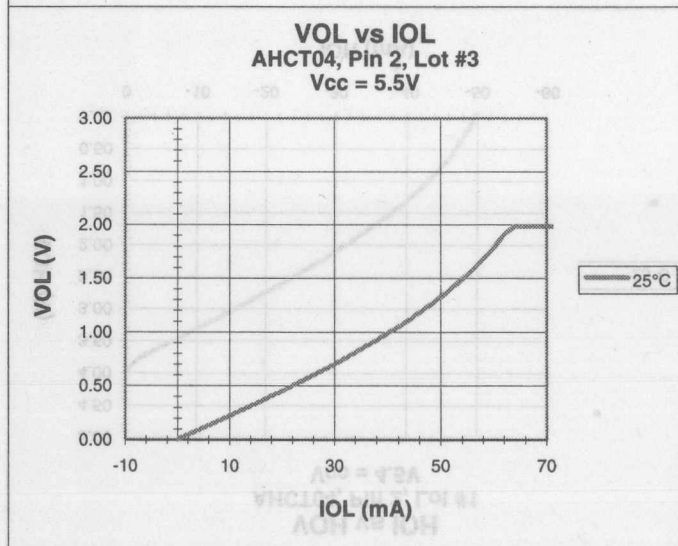
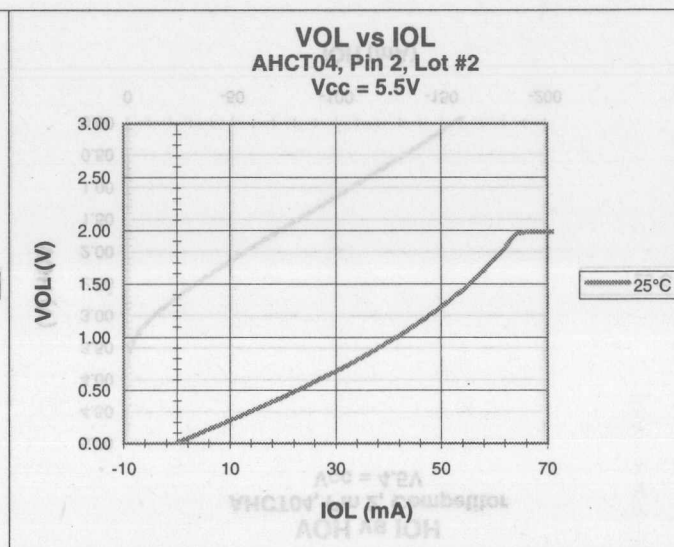
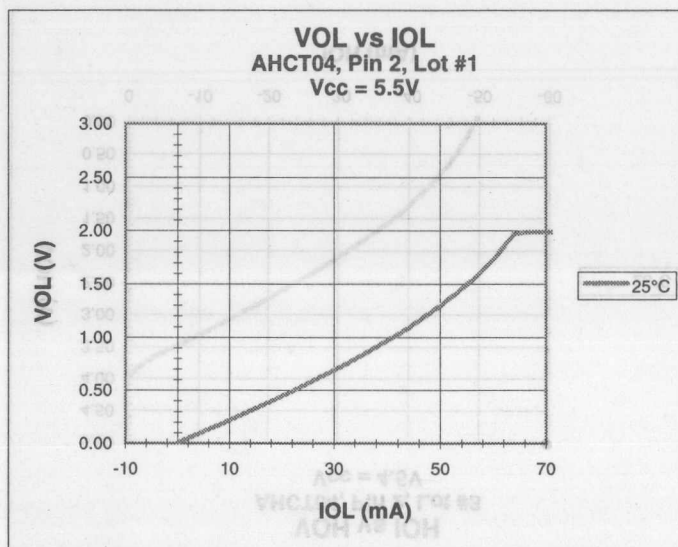


**VOL vs IOL**  
AHCT04, Pin 2, Lot #3  
Vcc = 4.5V



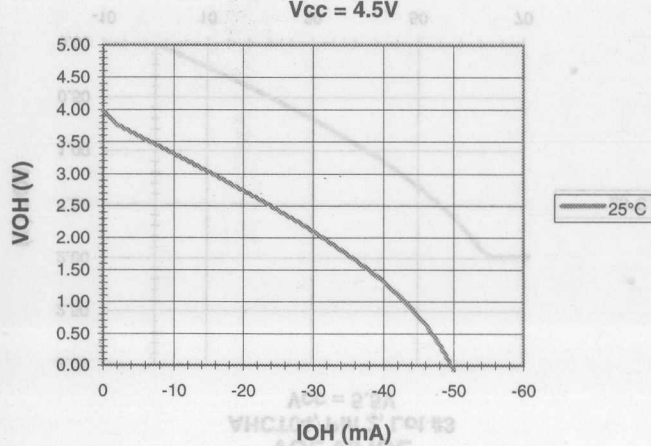
**VOL vs IOL**  
AHCT04, Pin 2, Competitor  
Vcc = 4.5V



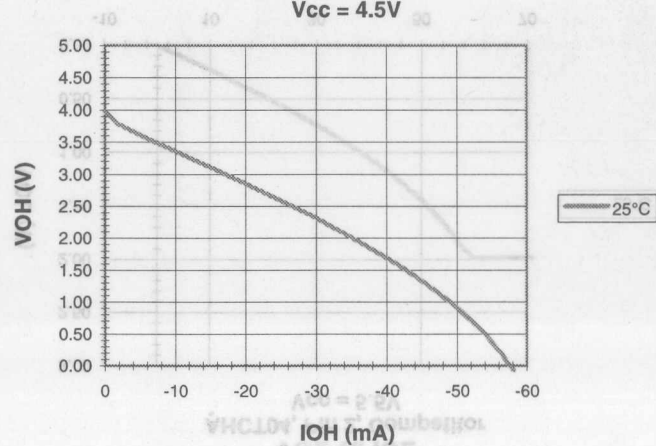




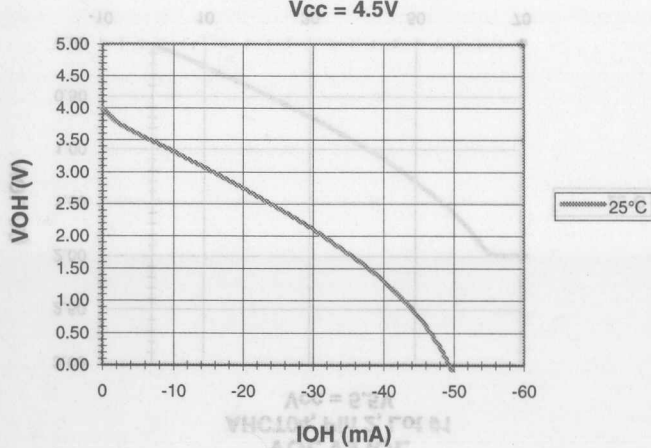
**VOH vs IOH**  
AHCT04, Pin 2, Lot #1  
Vcc = 4.5V



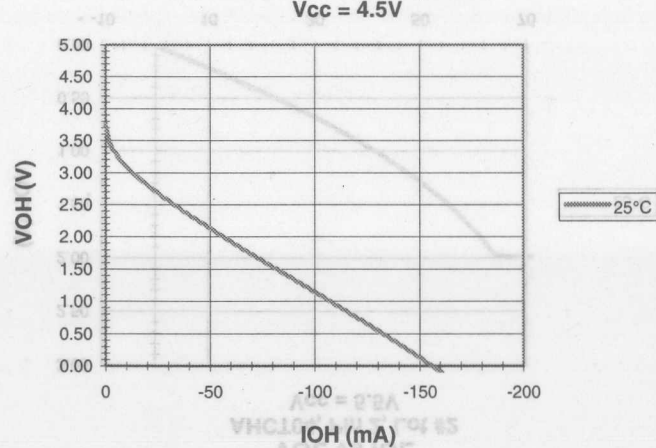
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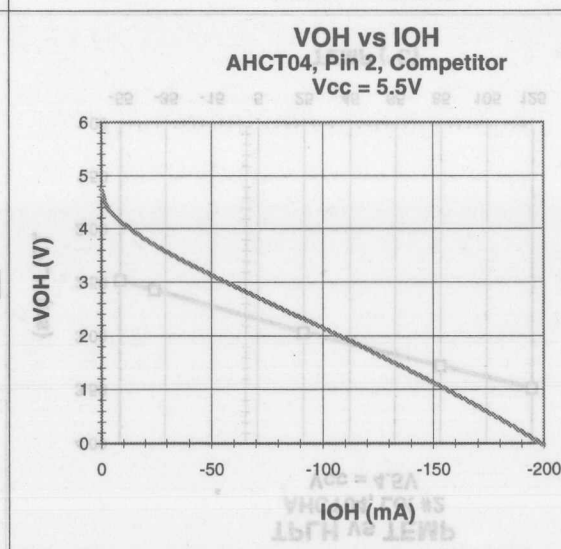
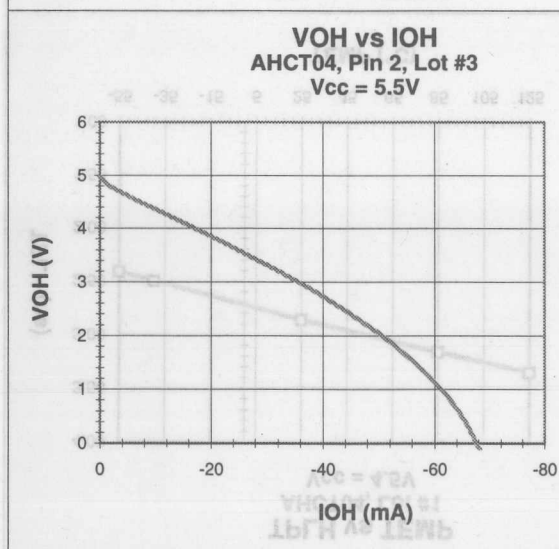
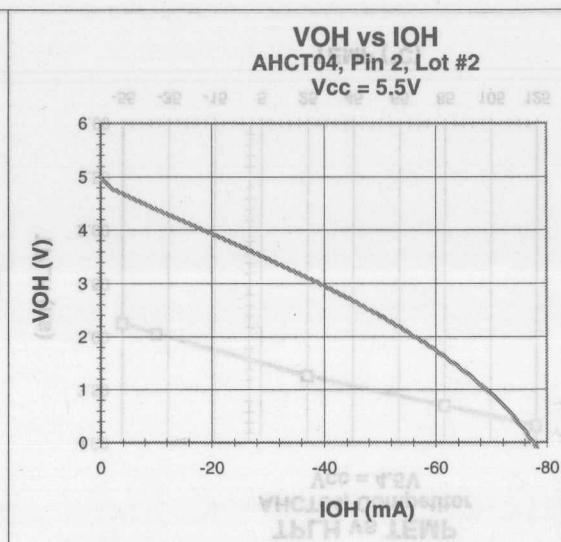
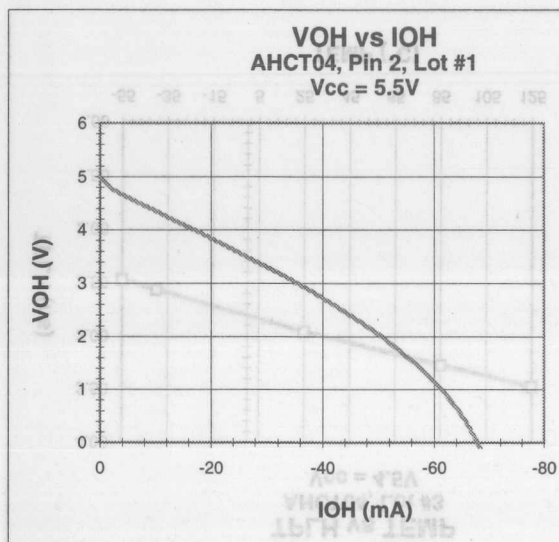


**VOH vs IOH**  
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Vcc = 4.5V

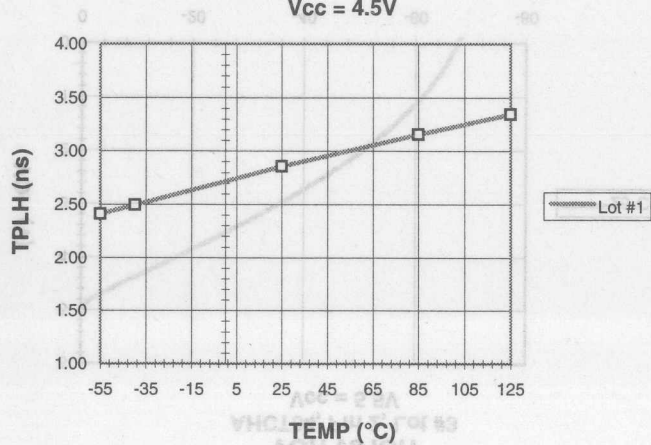


**VOH vs IOH**  
AHCT04, Pin 2, Competitor  
Vcc = 4.5V

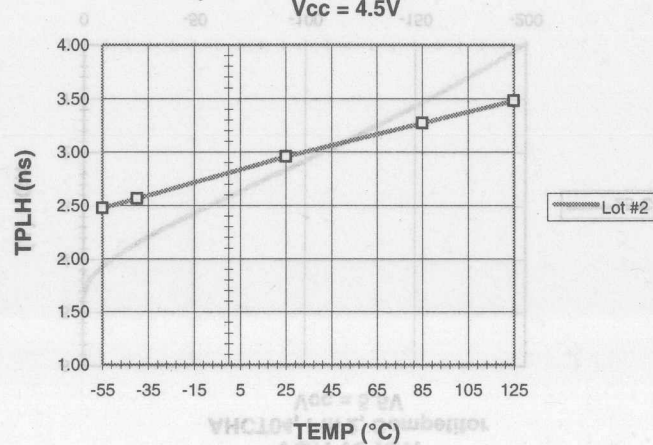




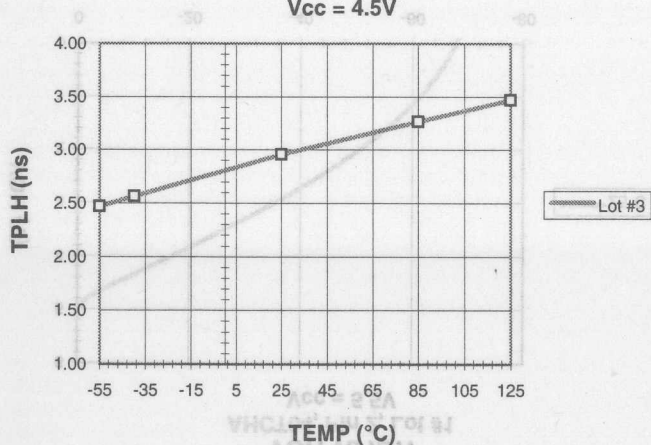
**TPLH vs TEMP**  
AHCT04, Lot #1  
Vcc = 4.5V



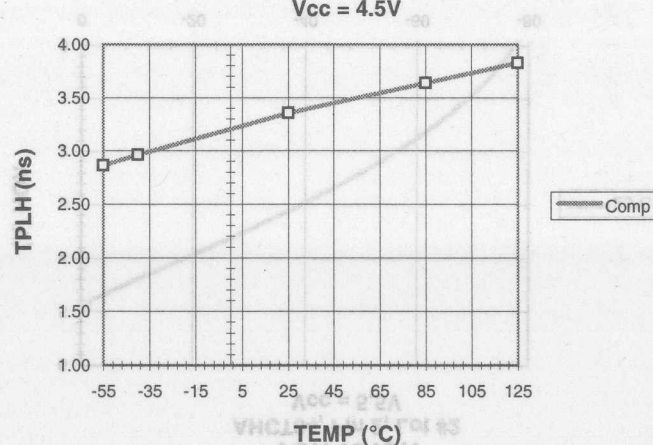
**TPLH vs TEMP**  
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Vcc = 4.5V

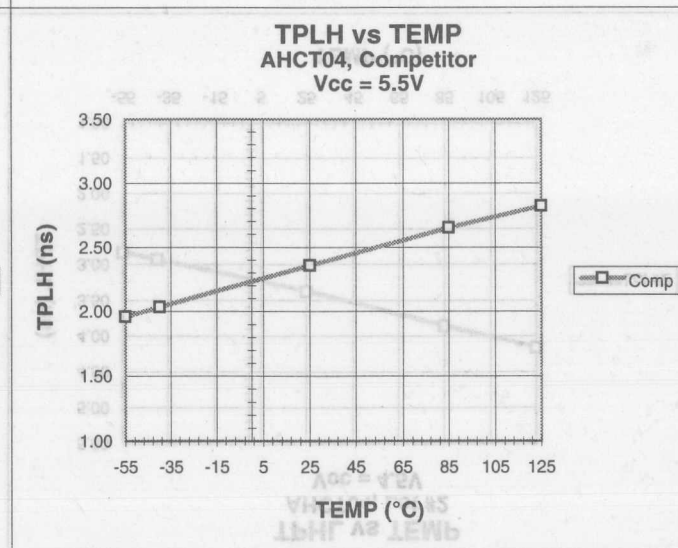
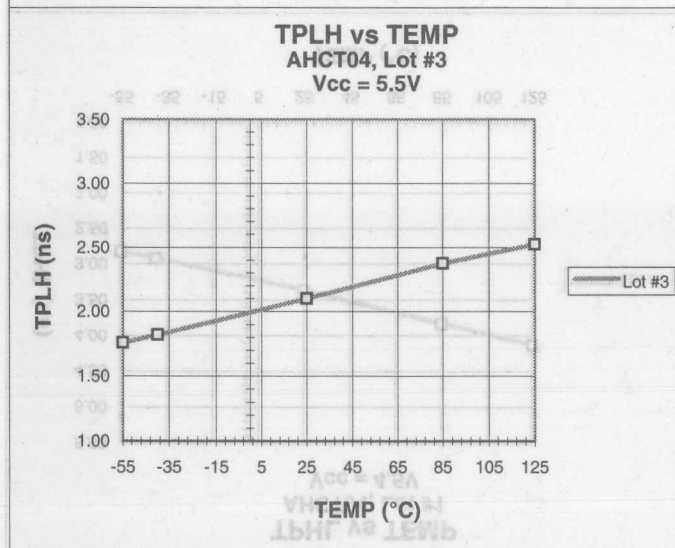
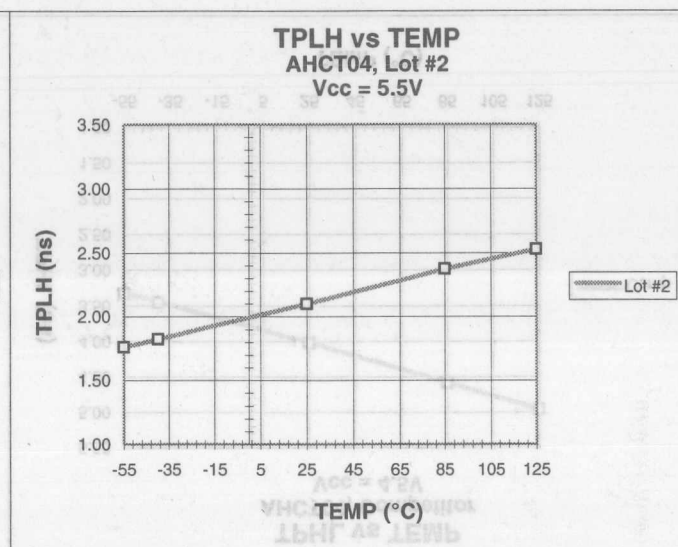
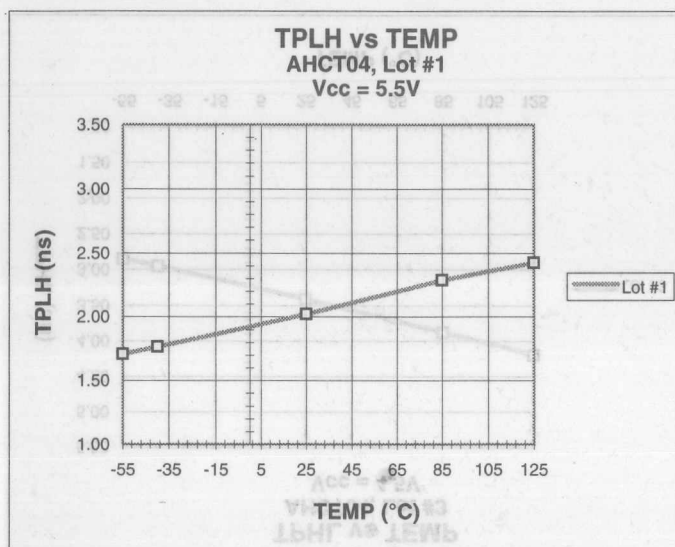


**TPLH vs TEMP**  
AHCT04, Lot #3  
Vcc = 4.5V

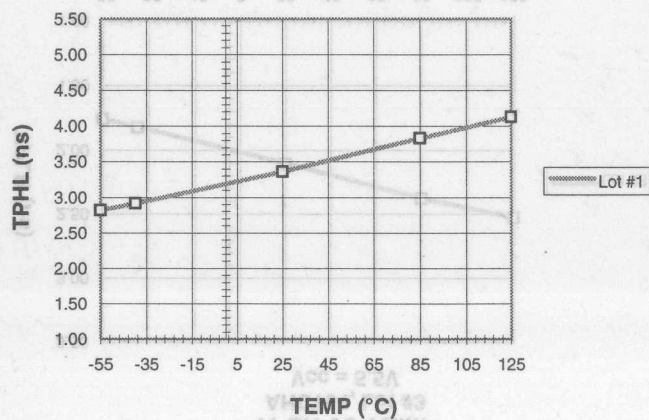


**TPLH vs TEMP**  
AHCT04, Competitor  
Vcc = 4.5V

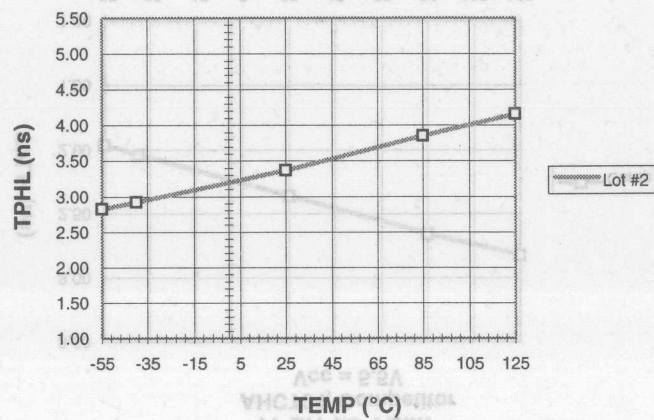




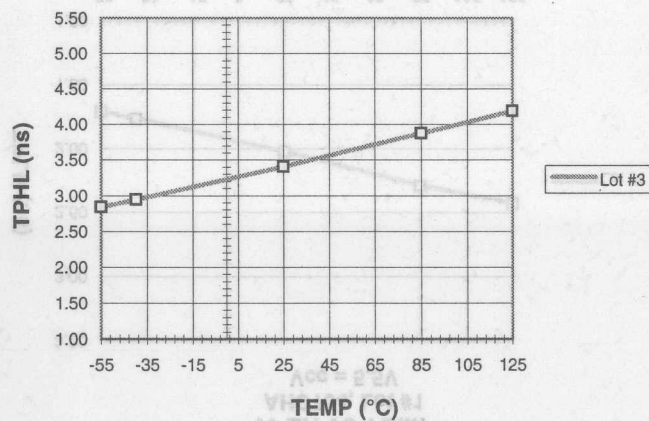
**TPHL vs TEMP**  
**AHCT04, Lot #1**  
**Vcc = 4.5V**



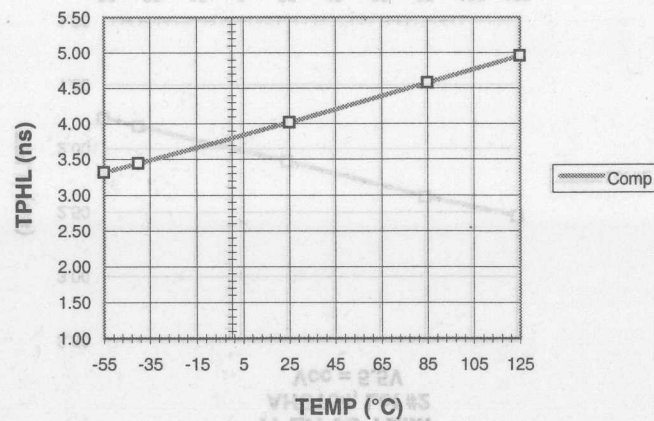
**TPHL vs TEMP**  
**AHCT04, Lot #2**  
**Vcc = 4.5V**



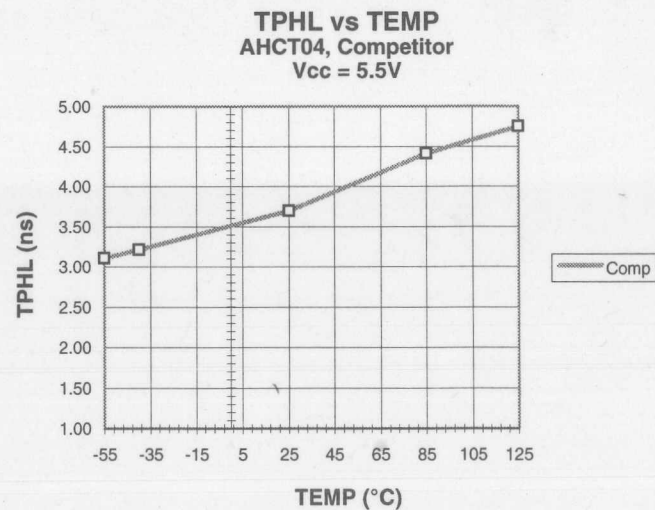
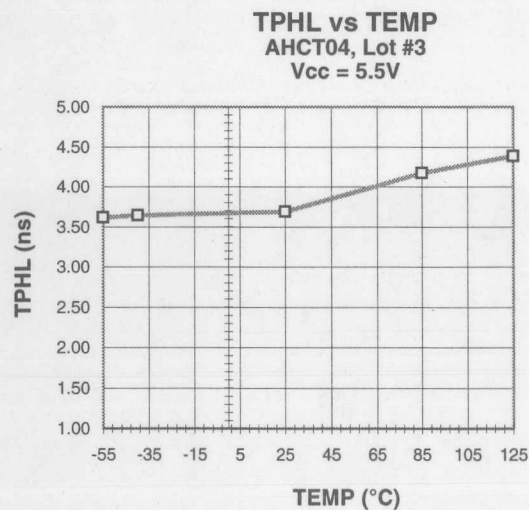
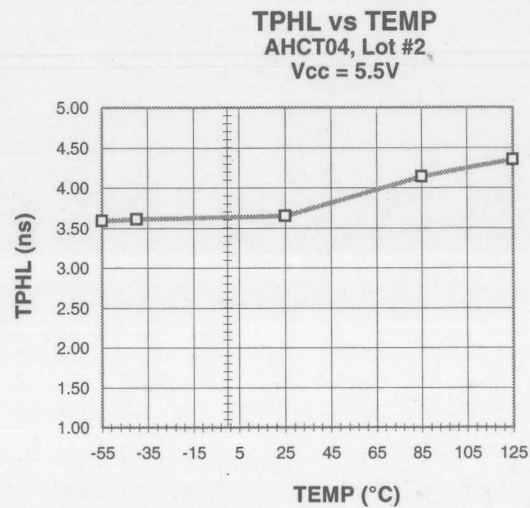
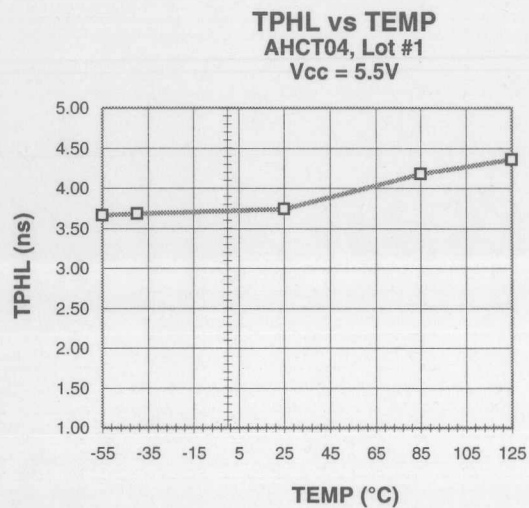
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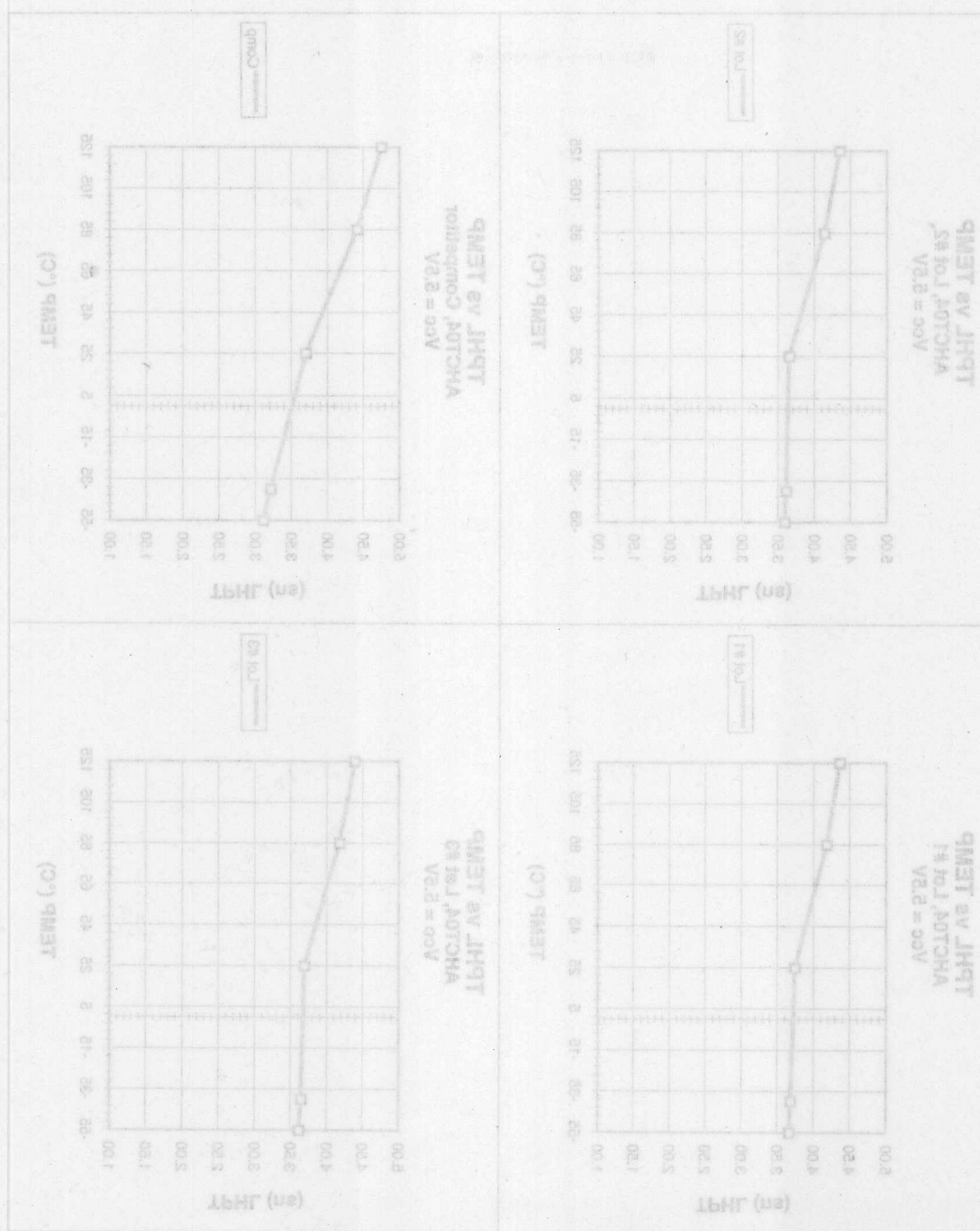


**TPHL vs TEMP**  
**AHCT04, Competitor**  
**Vcc = 4.5V**





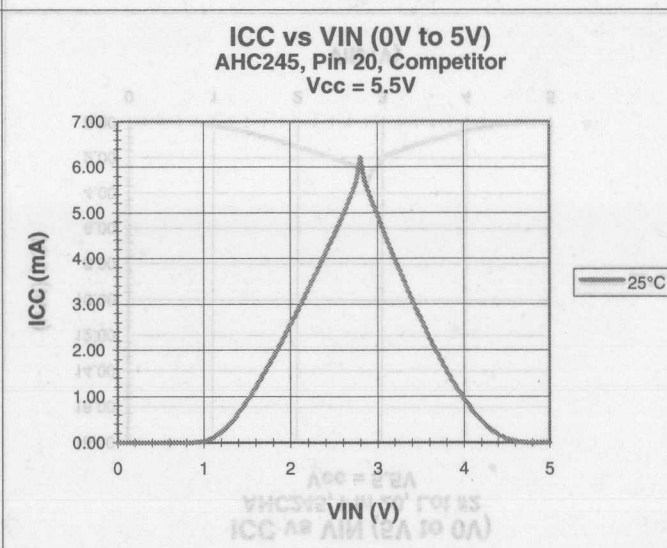
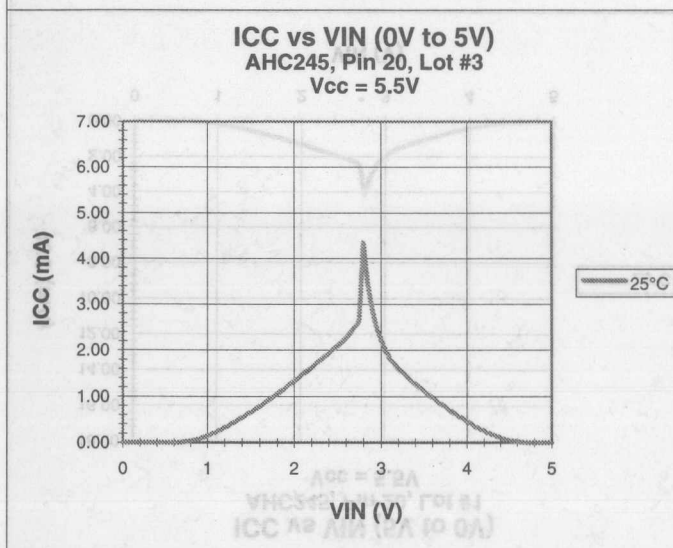
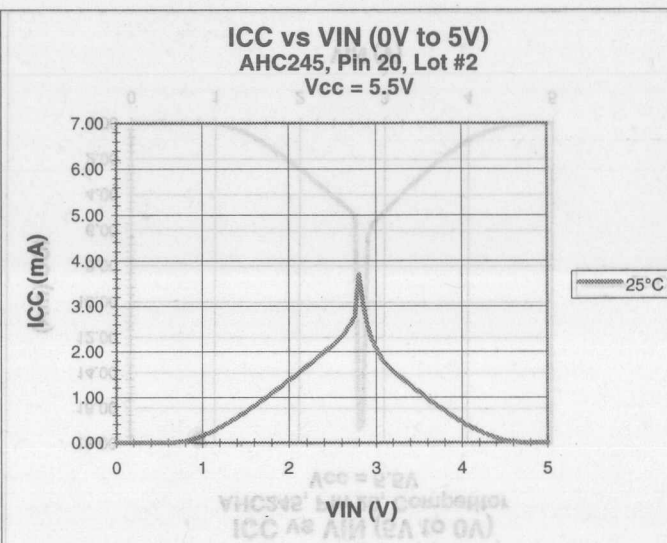
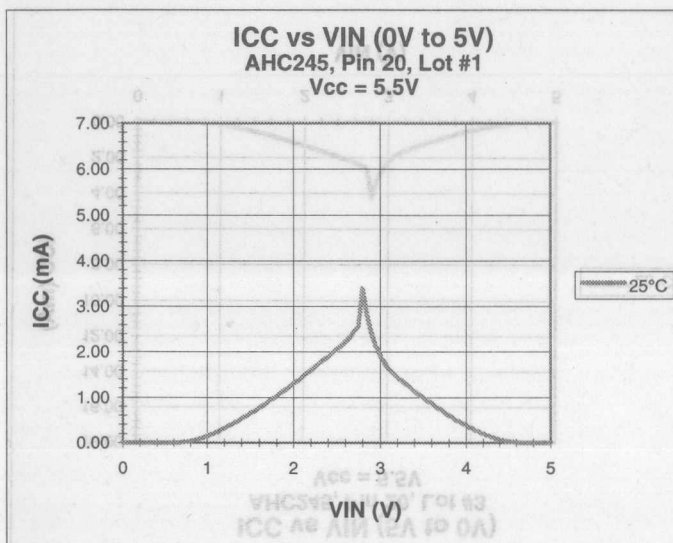




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AHCT04 Qualification Data	B
AHC245 Qualification Data	C
AHCT245 Qualification Data	D

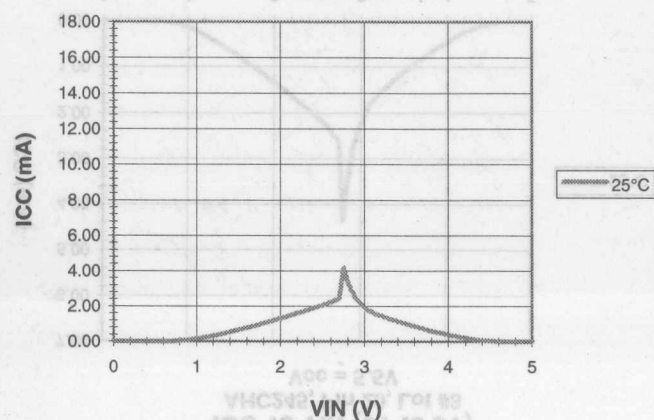
1	General Information
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4	Medical Data
A	AHC Qualification Data
B	AHC Qualification Data
C	AHC245 Qualification Data
	AHC245 Qualification Data

# AHC245 Qualification Data

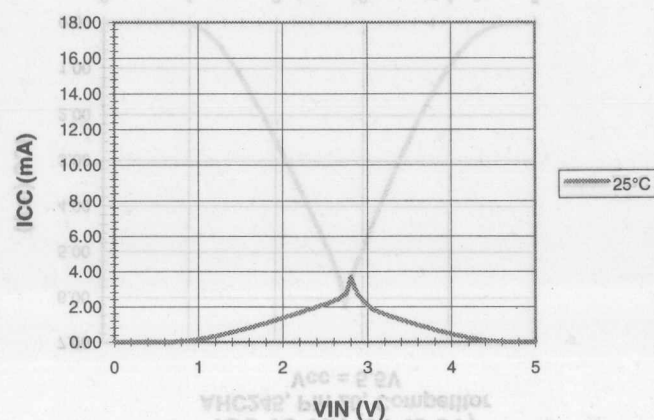




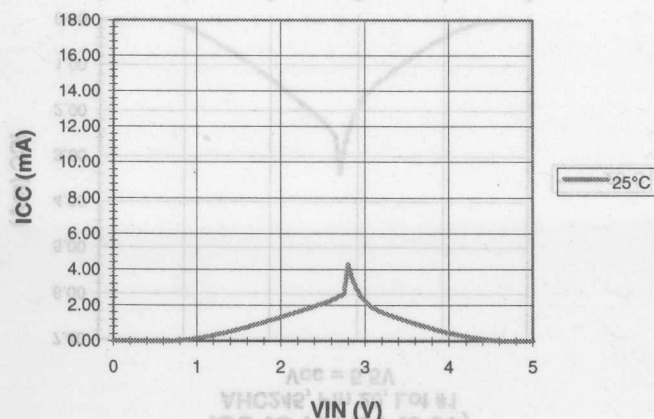
**ICC vs VIN (5V to 0V)**  
AHC245, Pin 20, Lot #1  
Vcc = 5.5V



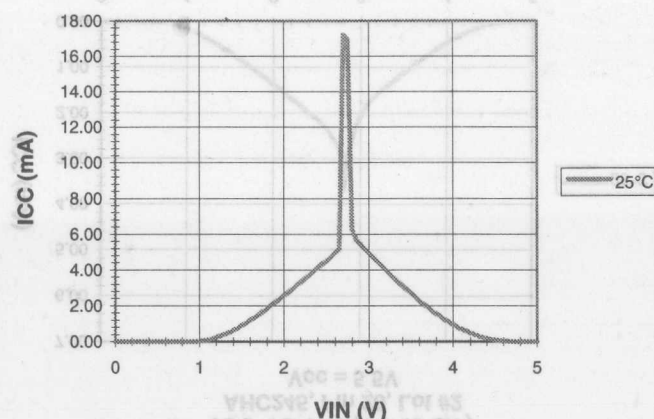
**ICC vs VIN (5V to 0V)**  
AHC245, Pin 20, Lot #2  
Vcc = 5.5V

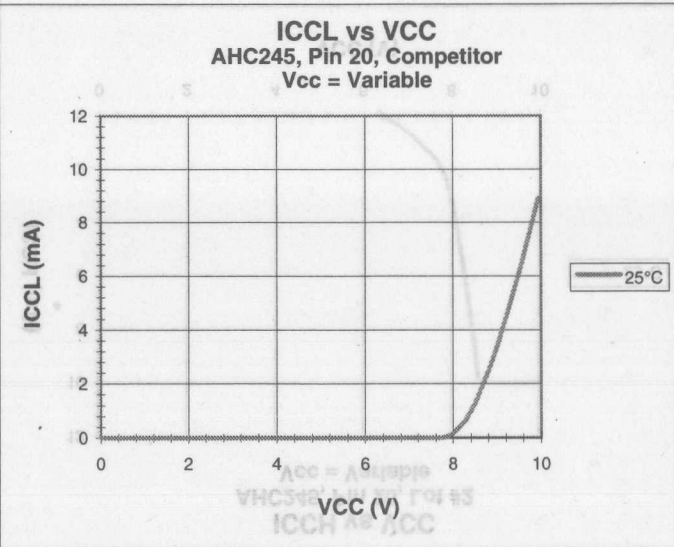
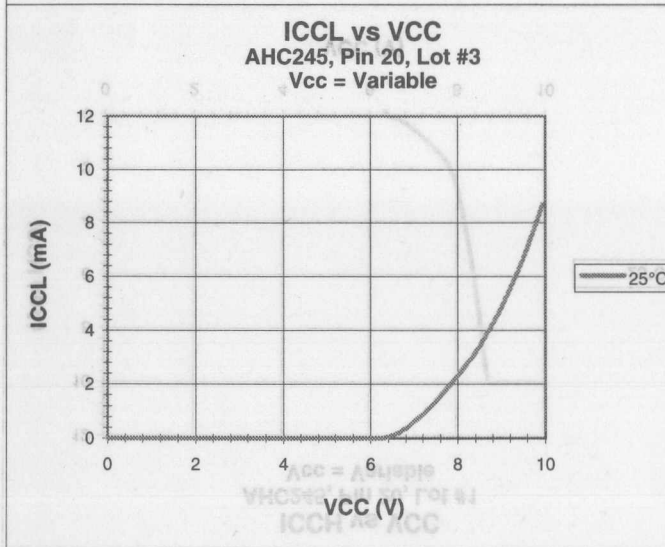
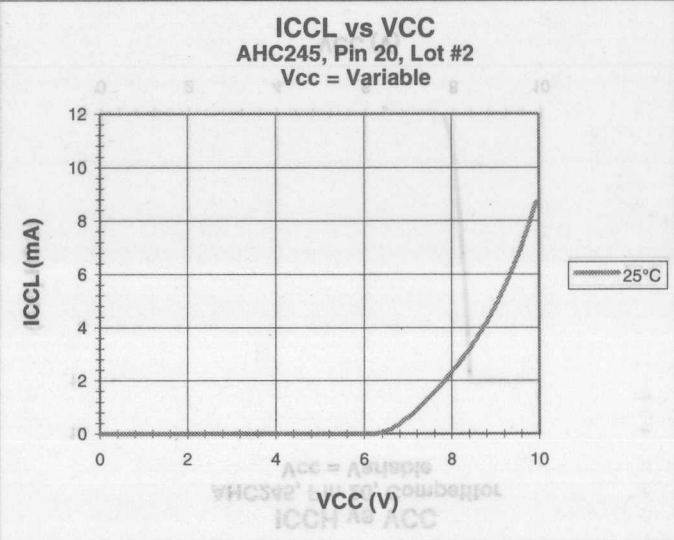
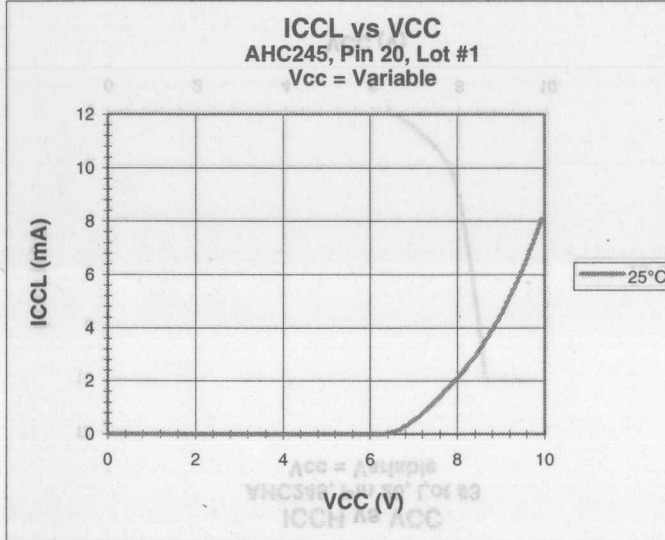


**ICC vs VIN (5V to 0V)**  
AHC245, Pin 20, Lot #3  
Vcc = 5.5V

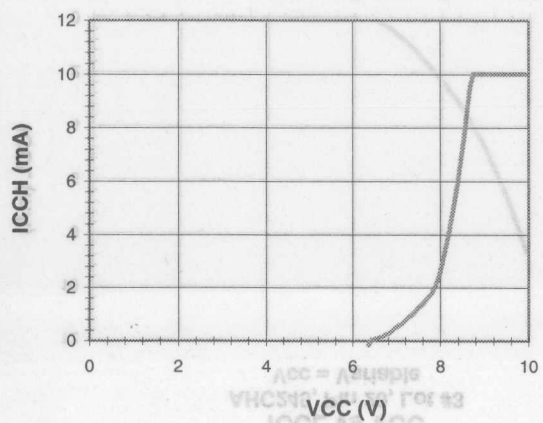


**ICC vs VIN (5V to 0V)**  
AHC245, Pin 20, Competitor  
Vcc = 5.5V

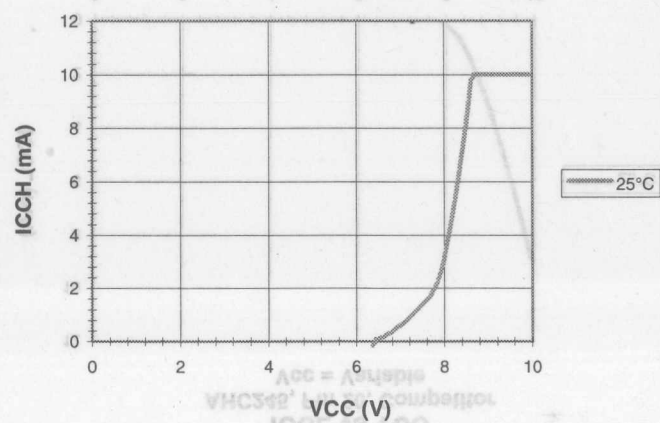




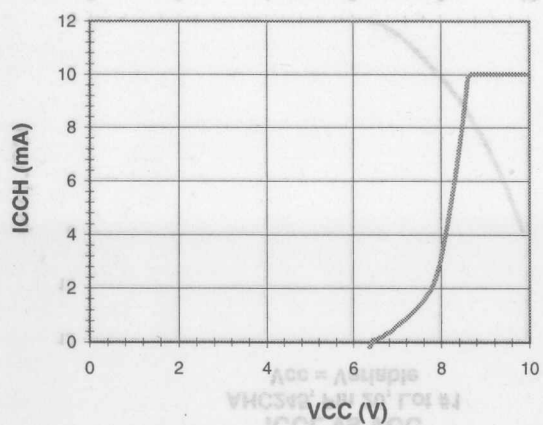
**ICCH vs VCC**  
AHC245, Pin 20, Lot #1  
Vcc = Variable



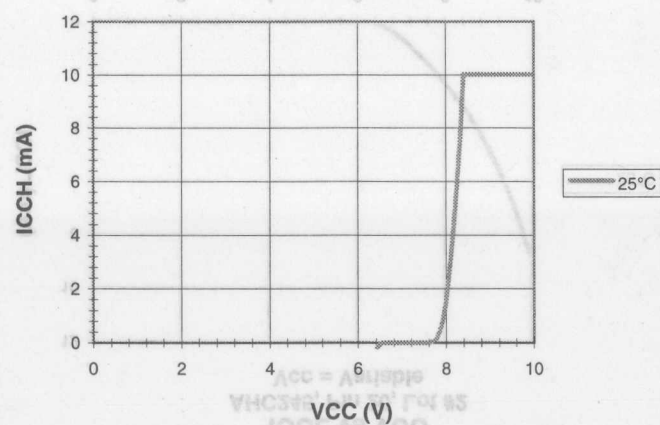
**ICCH vs VCC**  
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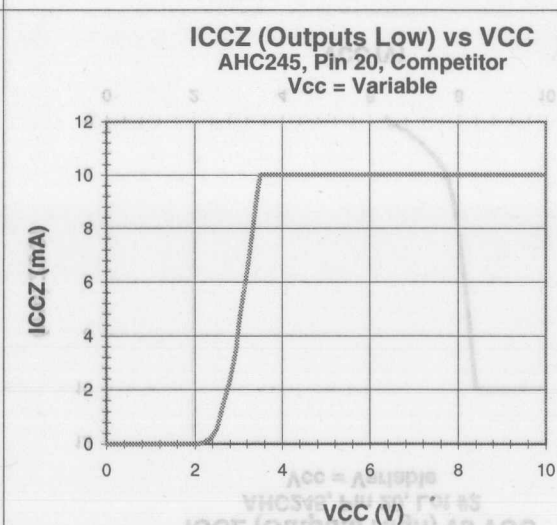
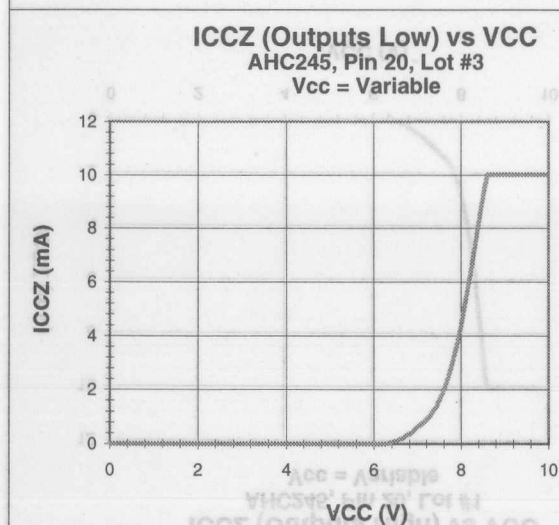
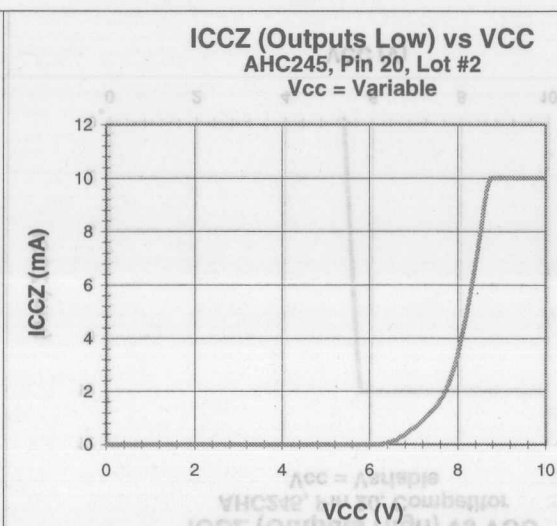
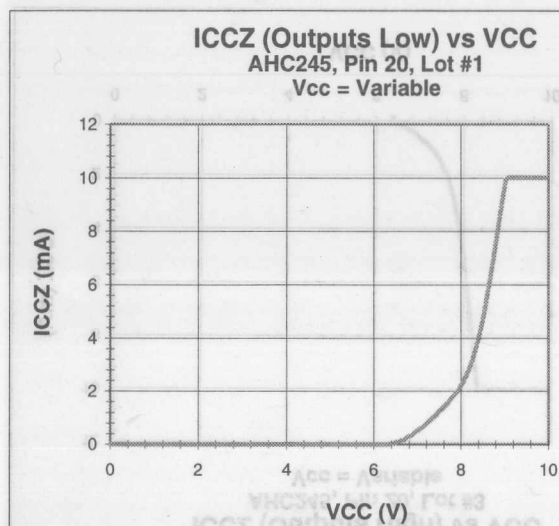


**ICCH vs VCC**  
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Vcc = Variable

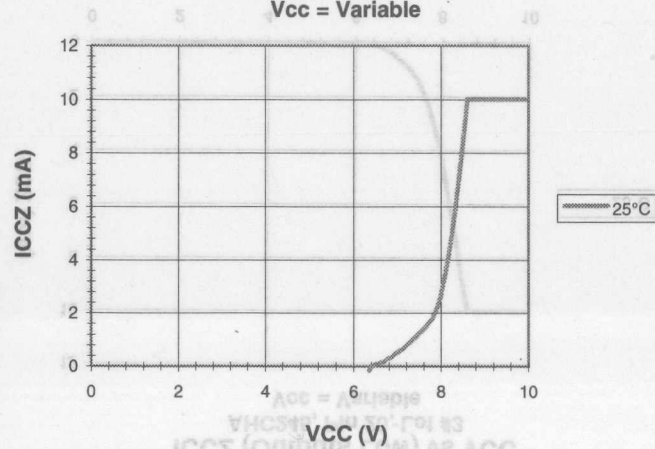


**ICCH vs VCC**  
AHC245, Pin 20, Competitor  
Vcc = Variable

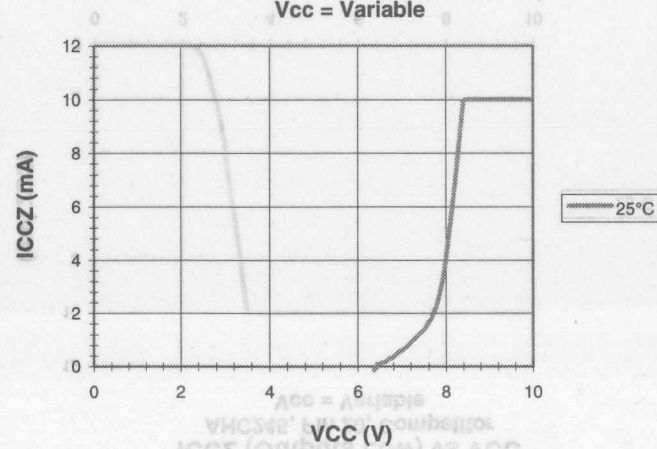




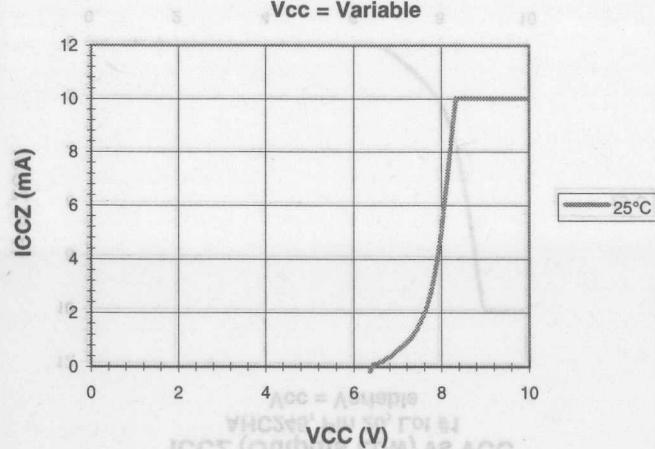
**ICCZ (Outputs High) vs VCC**  
AHC245, Pin 20, Lot #1  
Vcc = Variable



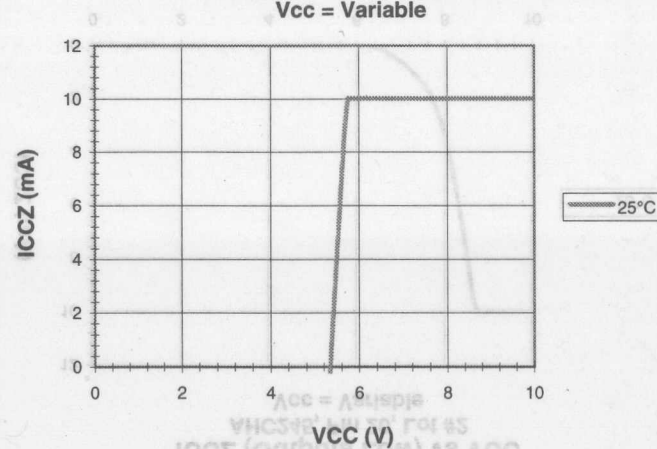
**ICCZ (Outputs High) vs VCC**  
AHC245, Pin 20, Lot #2  
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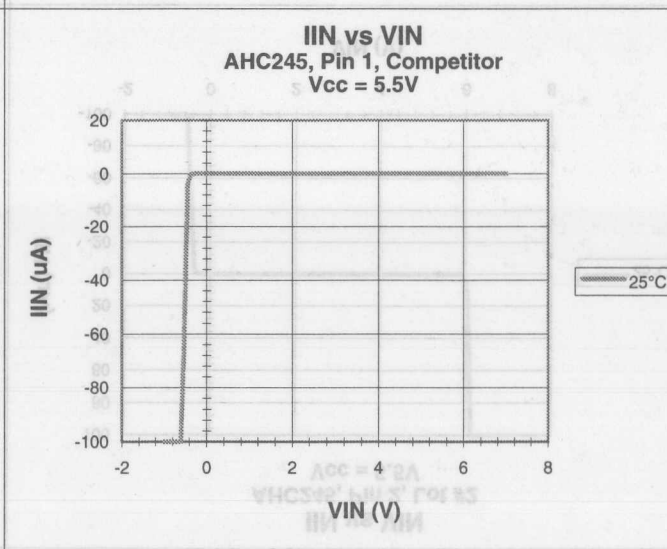
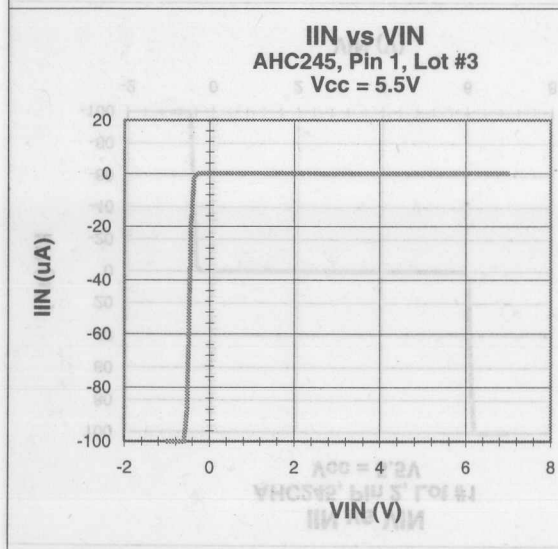
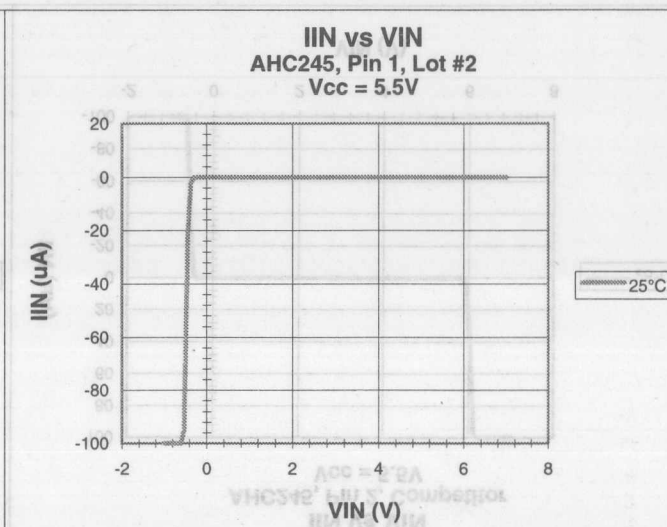
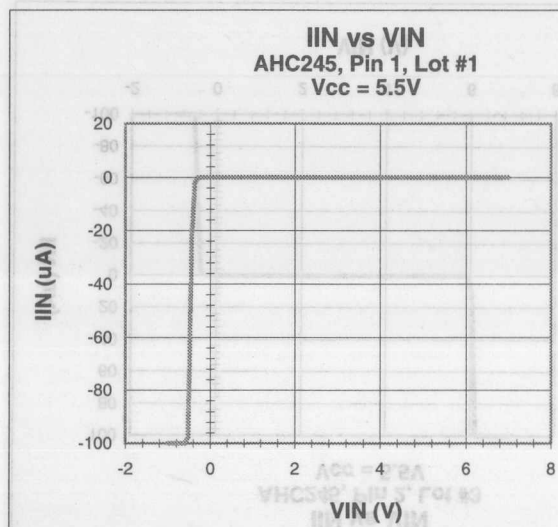
**ICCZ (Outputs High) vs VCC**  
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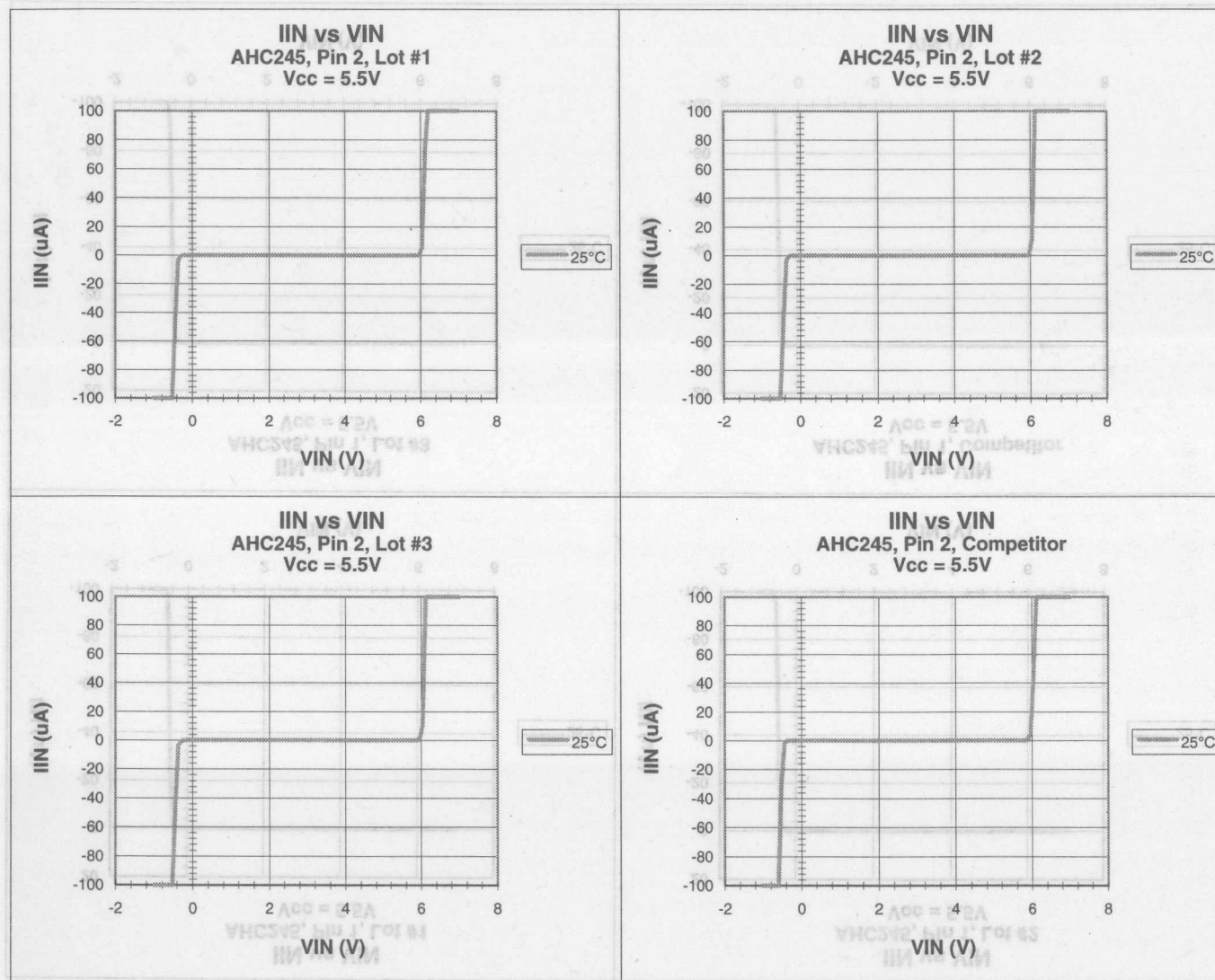


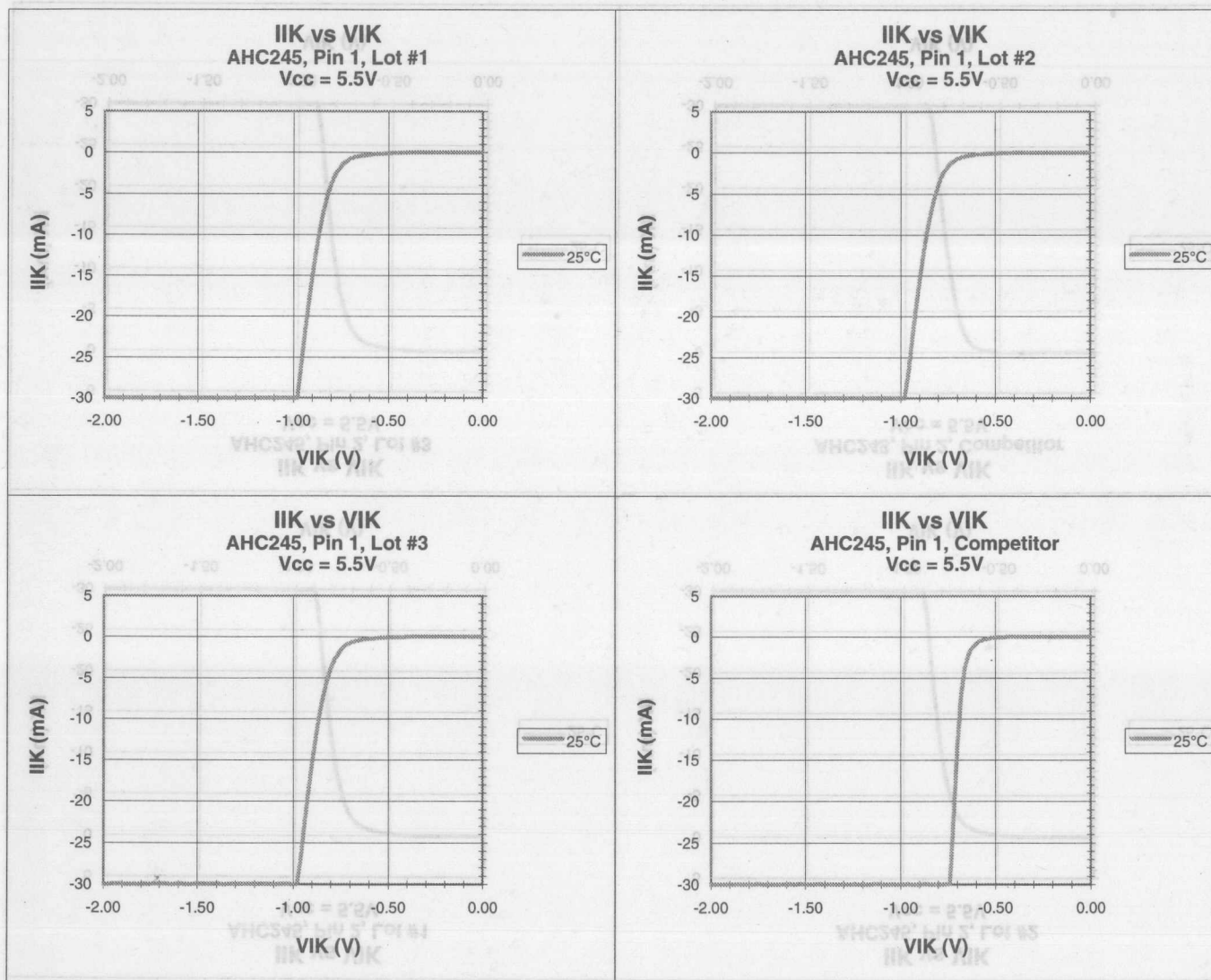
**ICCZ (Outputs High) vs VCC**  
AHC245, Pin 20, Competitor  
Vcc = Variable

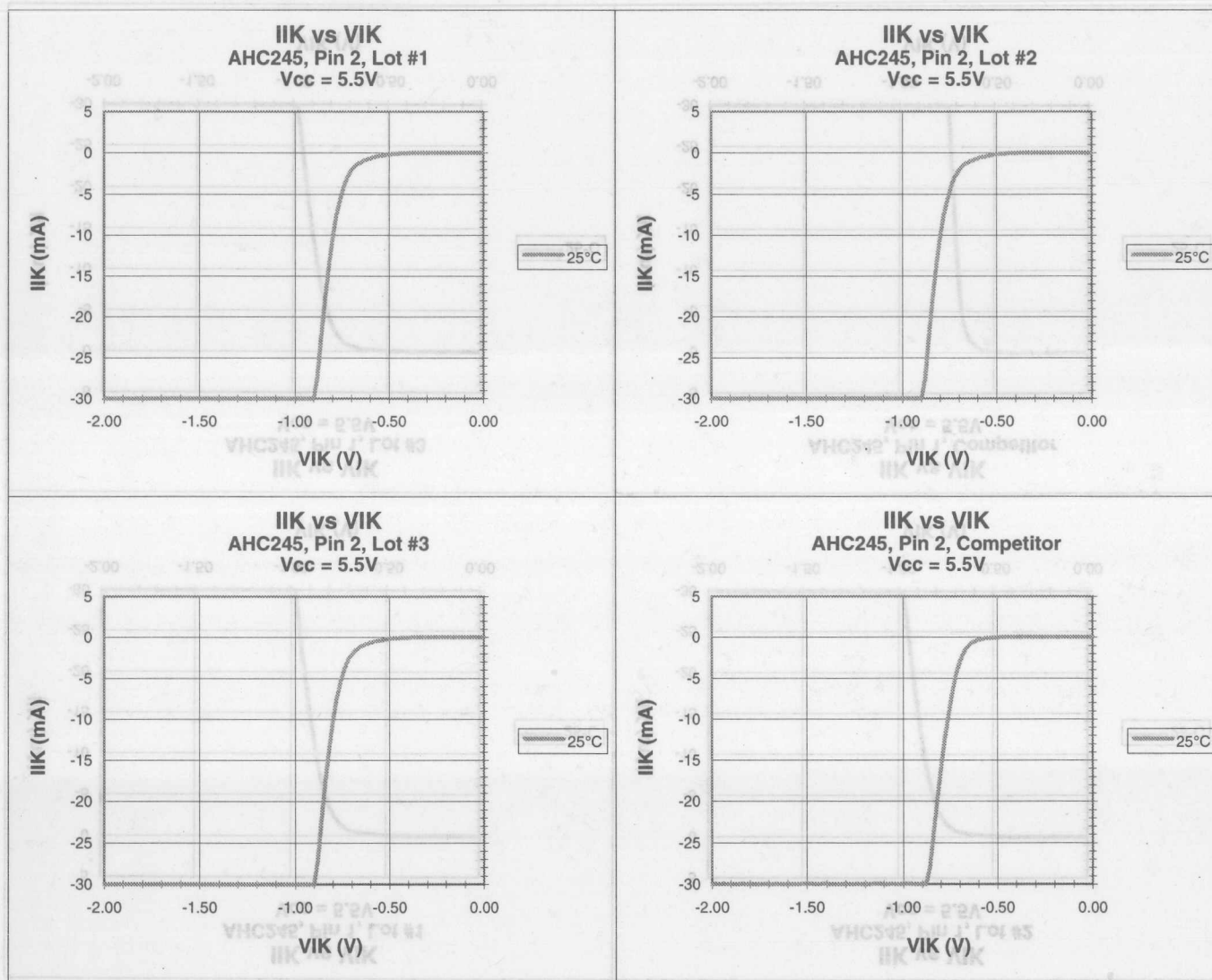


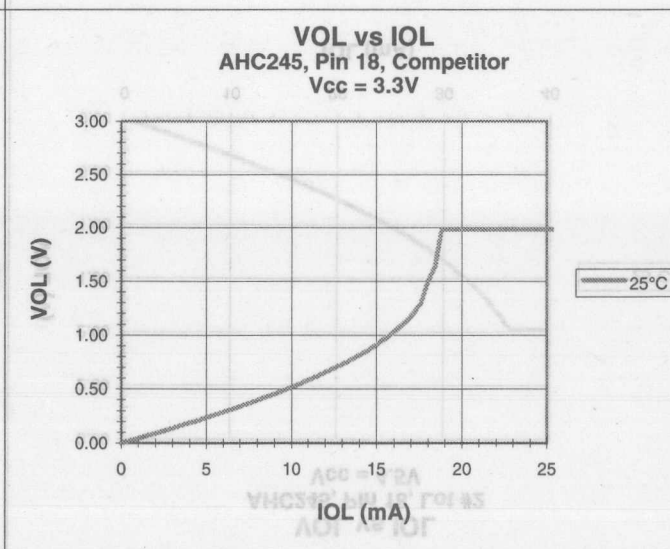
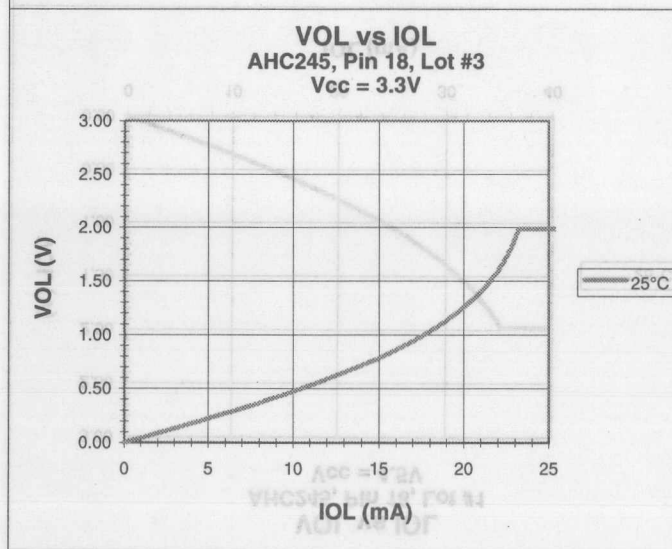
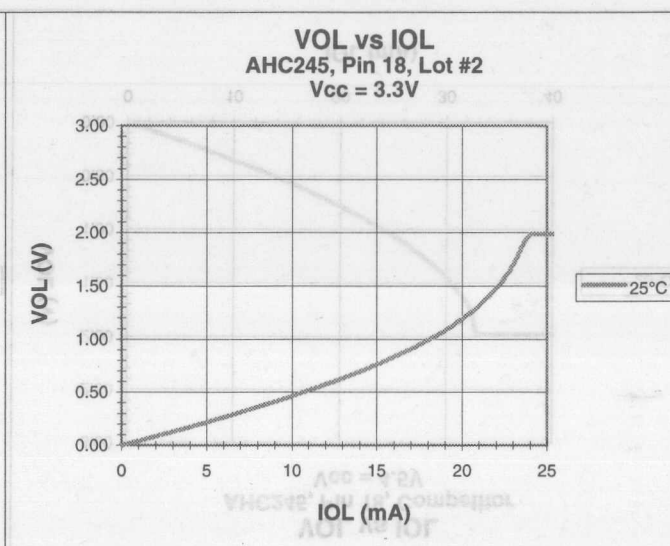
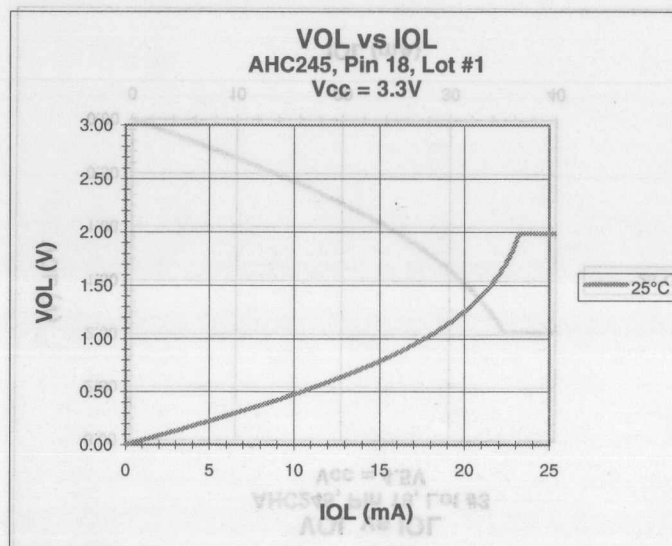




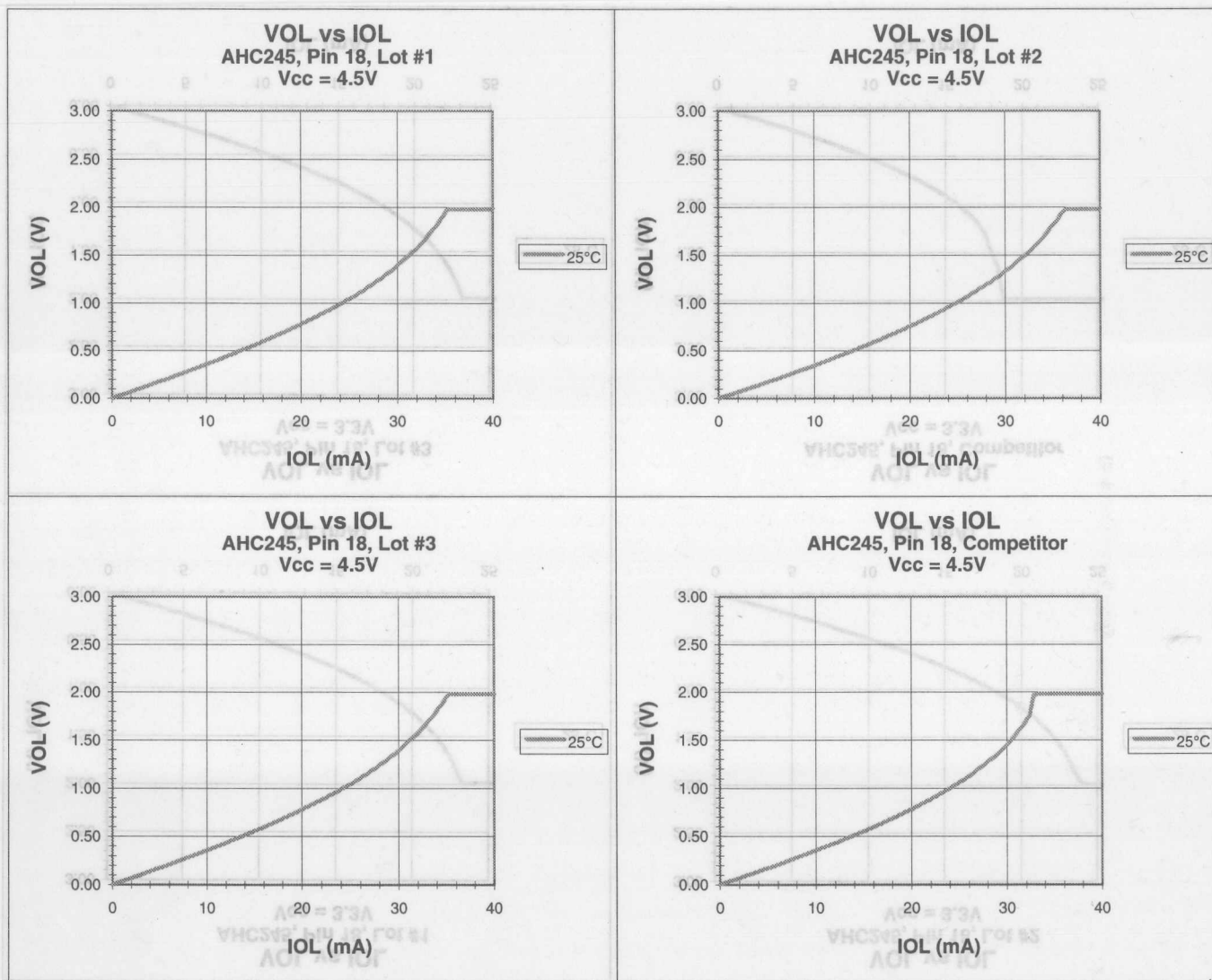


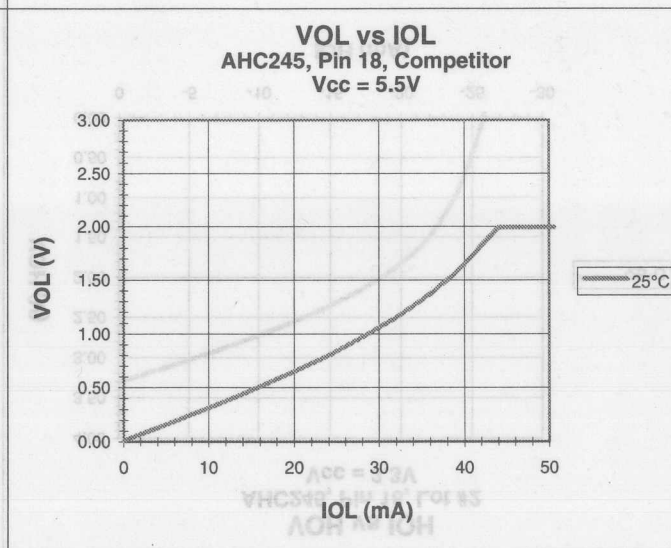
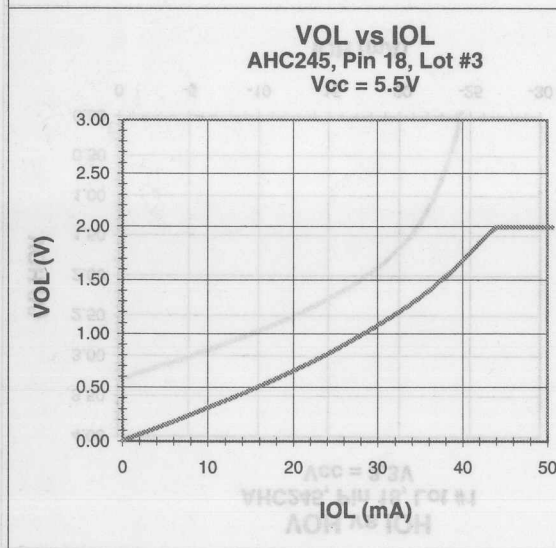
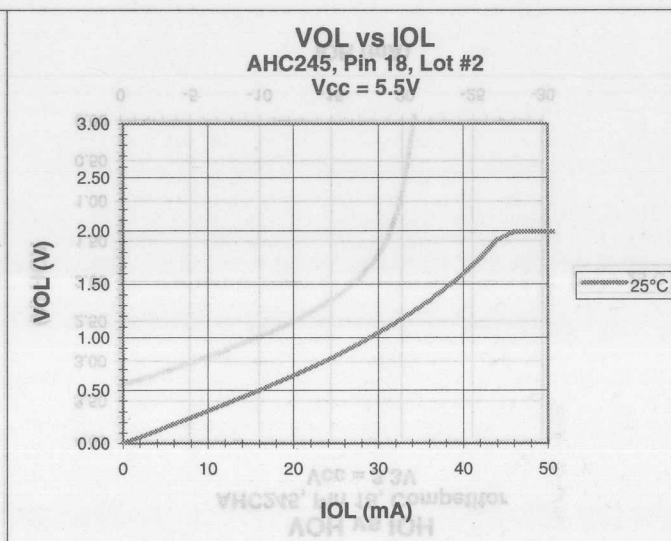
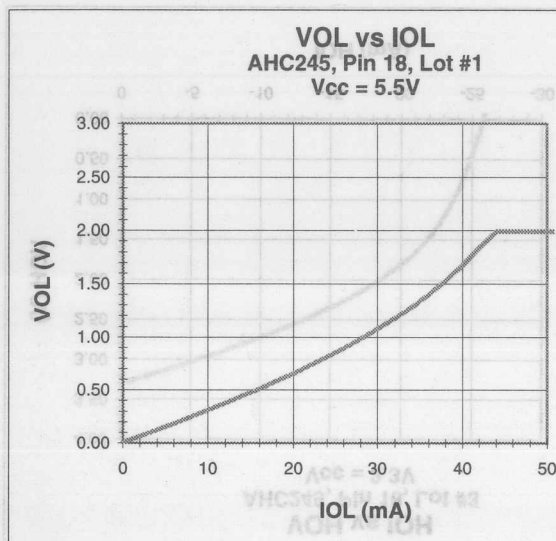




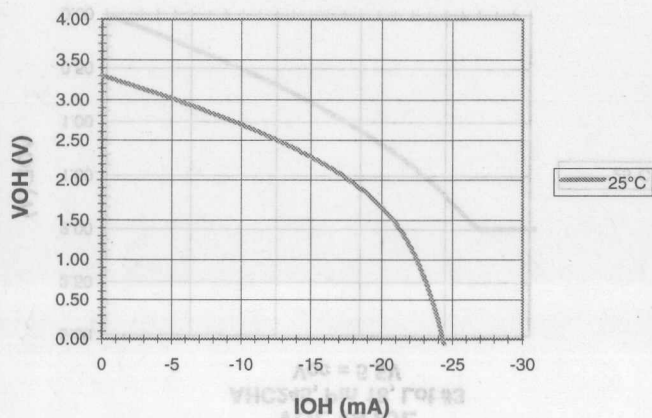




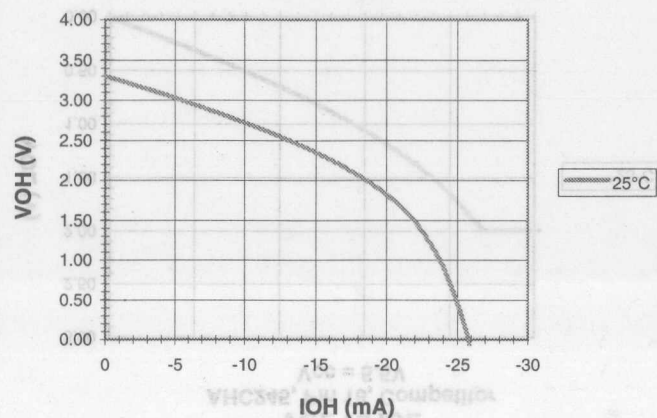




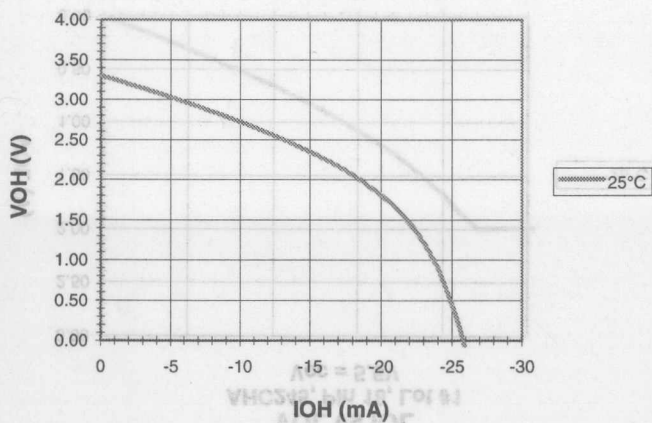
**VOH vs IOH**  
AHC245, Pin 18, Lot #1  
Vcc = 3.3V



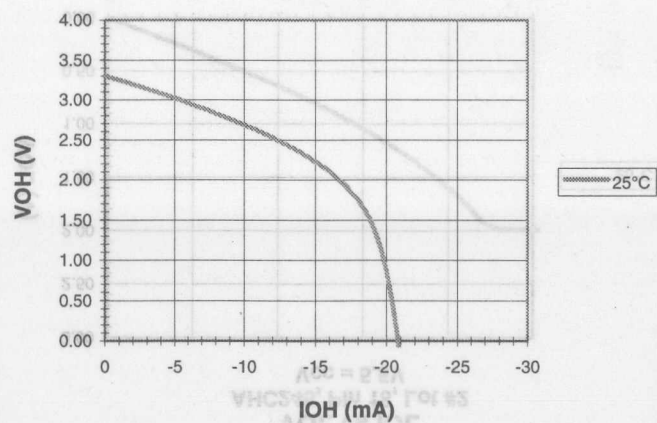
**VOH vs IOH**  
AHC245, Pin 18, Lot #2  
Vcc = 3.3V

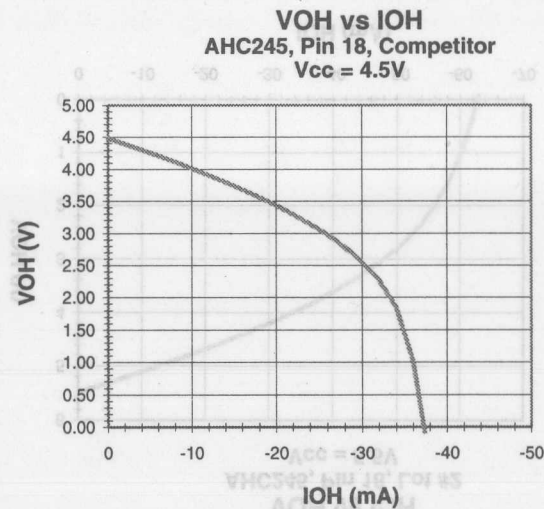
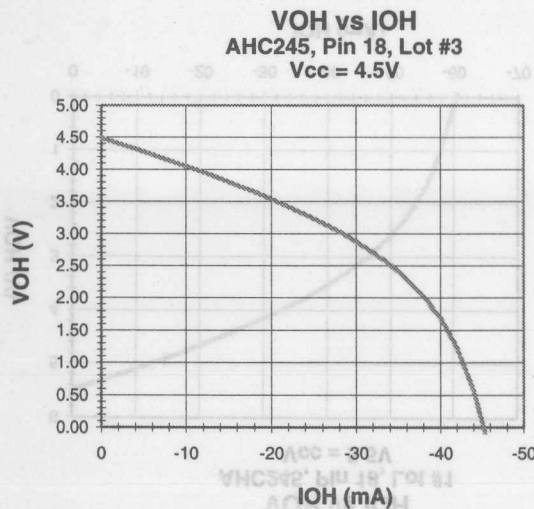
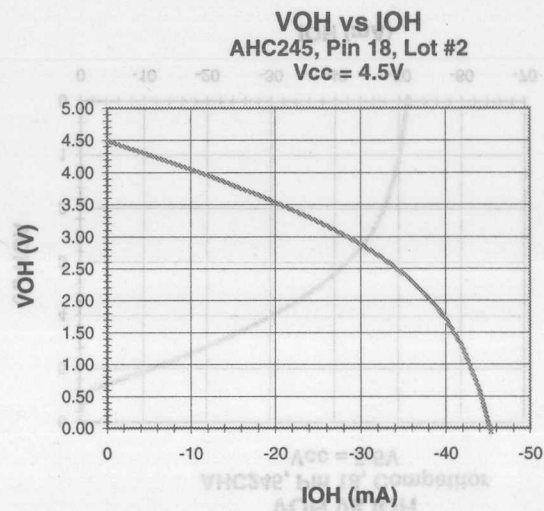
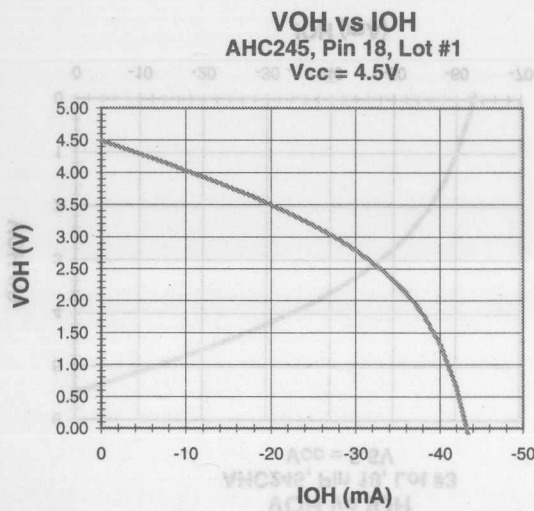


**VOH vs IOH**  
AHC245, Pin 18, Lot #3  
Vcc = 3.3V

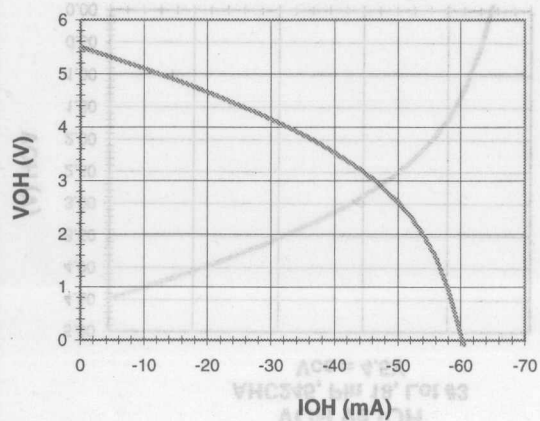


**VOH vs IOH**  
AHC245, Pin 18, Competitor  
Vcc = 3.3V

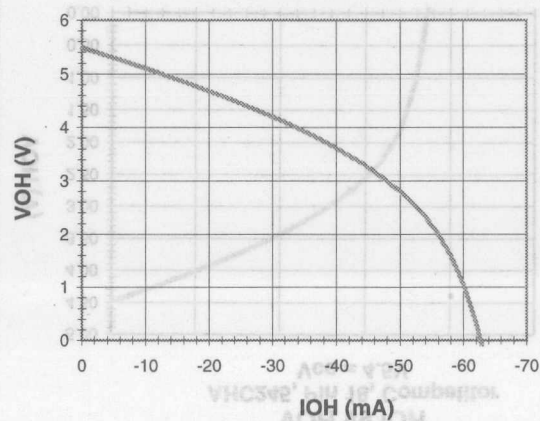




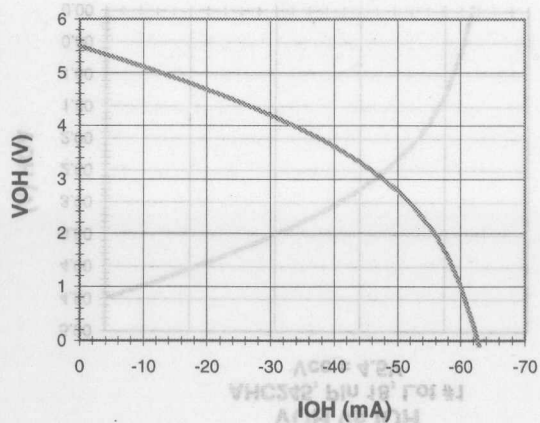
**VOH vs IOH**  
AHC245, Pin 18, Lot #1  
Vcc = 5.5V



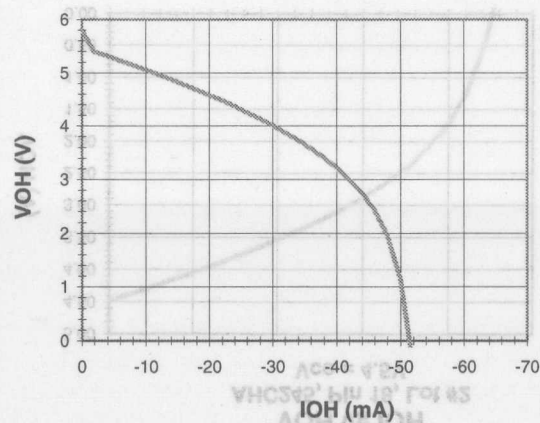
**VOH vs IOH**  
AHC245, Pin 18, Lot #2  
Vcc = 5.5V



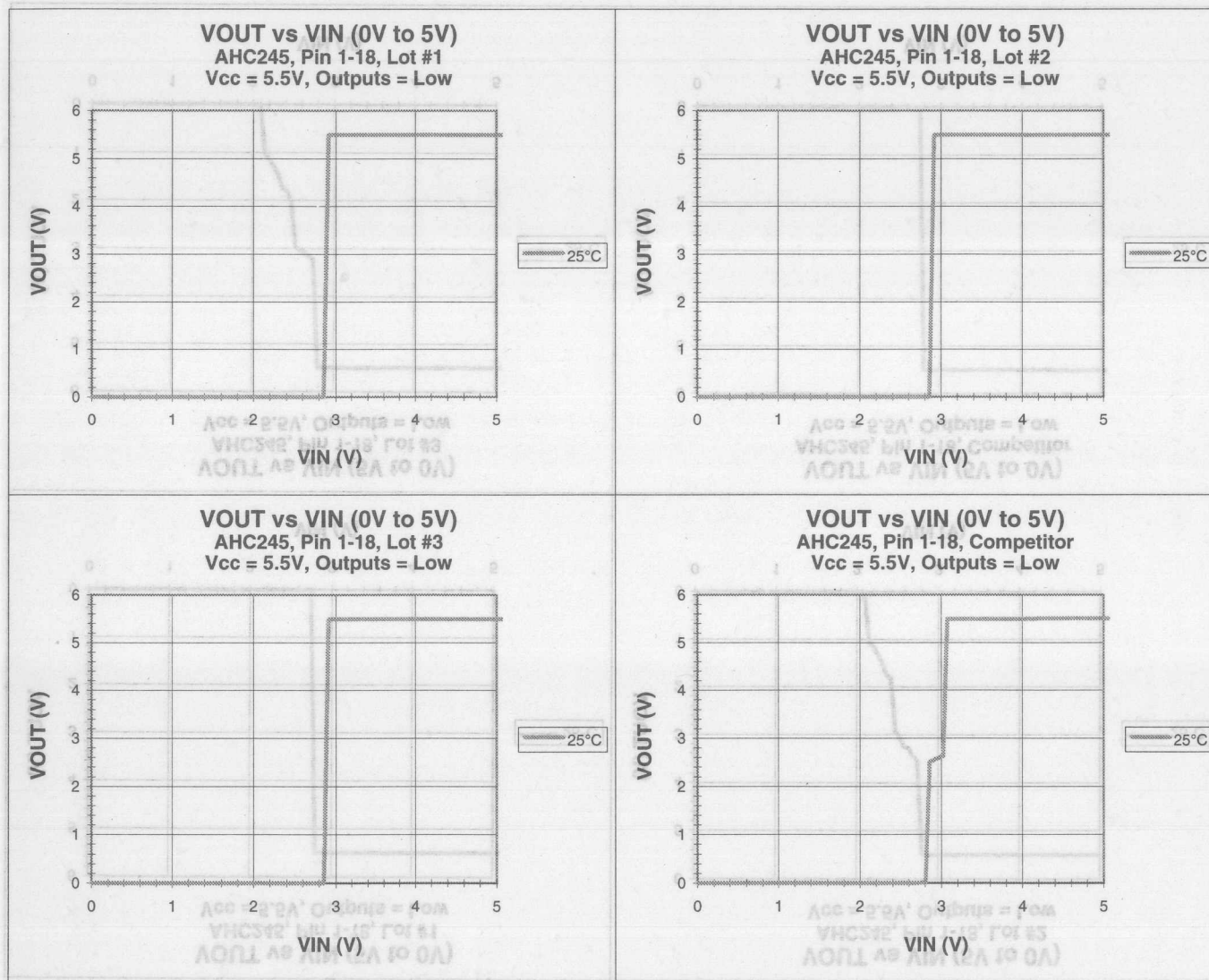
**VOH vs IOH**  
AHC245, Pin 18, Lot #3  
Vcc = 5.5V



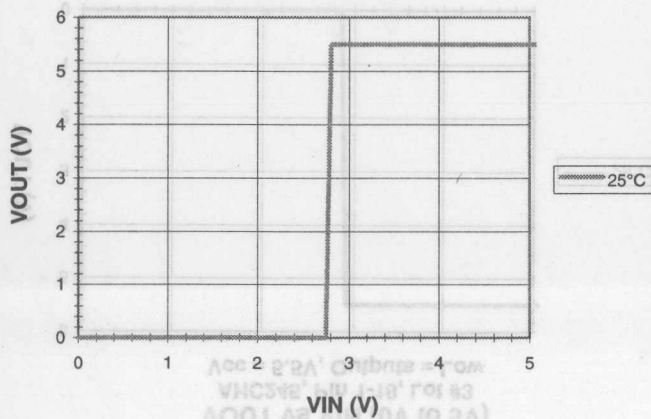
**VOH vs IOH**  
AHC245, Pin 18, Competitor  
Vcc = 5.5V



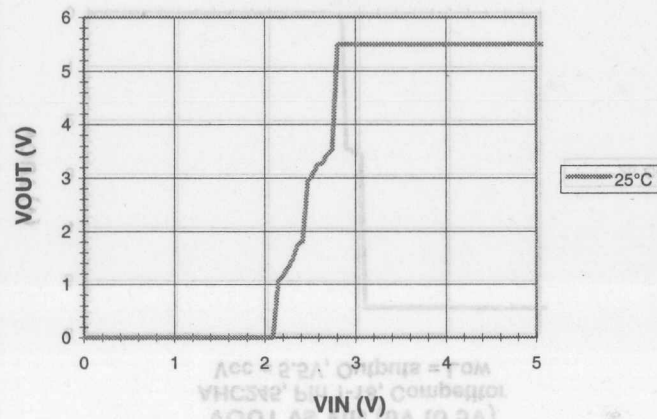




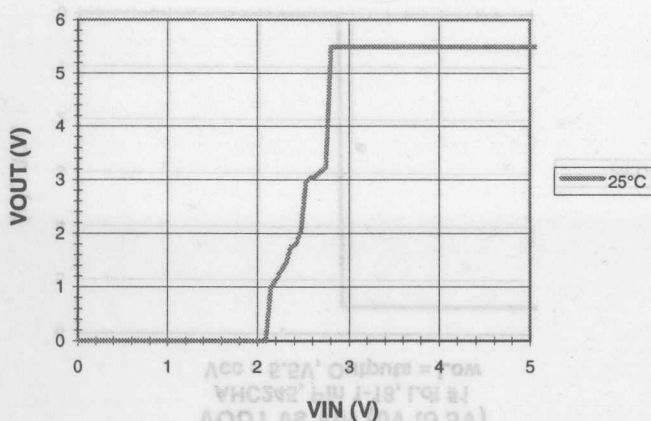
**VOUT vs VIN (5V to 0V)**  
AHC245, Pin 1-18, Lot #1  
Vcc = 5.5V, Outputs = Low



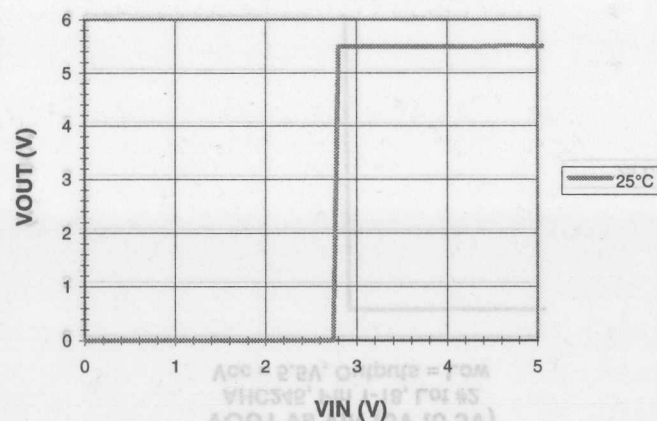
**VOUT vs VIN (5V to 0V)**  
AHC245, Pin 1-18, Lot #2  
Vcc = 5.5V, Outputs = Low



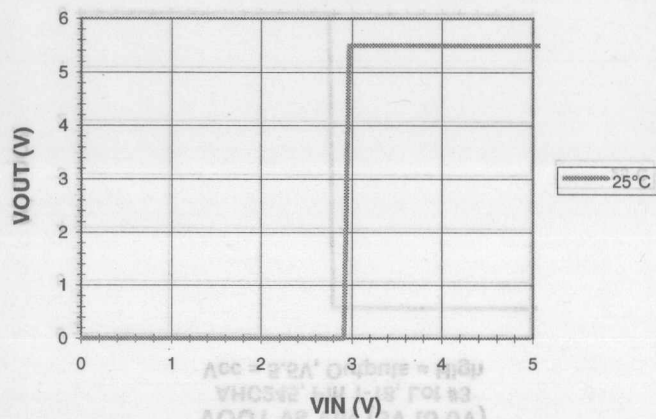
**VOUT vs VIN (5V to 0V)**  
AHC245, Pin 1-18, Lot #3  
Vcc = 5.5V, Outputs = Low



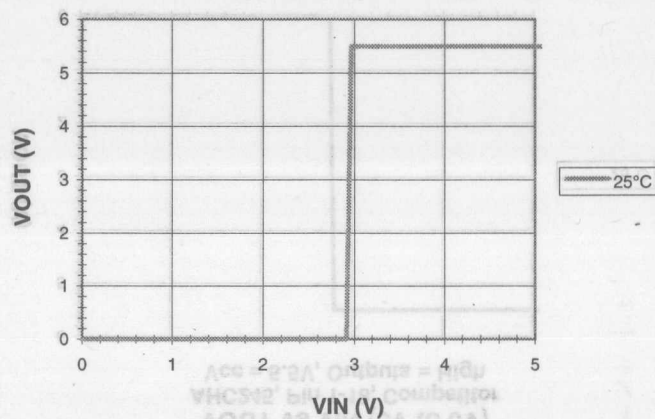
**VOUT vs VIN (5V to 0V)**  
AHC245, Pin 1-18, Competitor  
Vcc = 5.5V, Outputs = Low



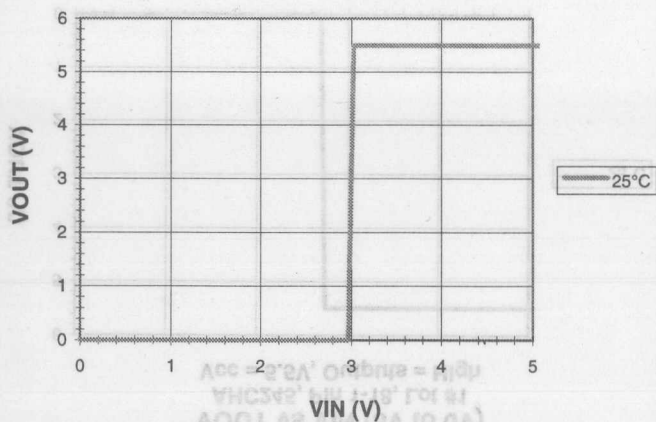
**VOUT vs VIN (0V to 5V)**  
**AHC245, Pin 1-18, Lot #1**  
**Vcc = 5.5V, Outputs = High**



**VOUT vs VIN (0V to 5V)**  
**AHC245, Pin 1-18, Lot #2**  
**Vcc = 5.5V, Outputs = High**



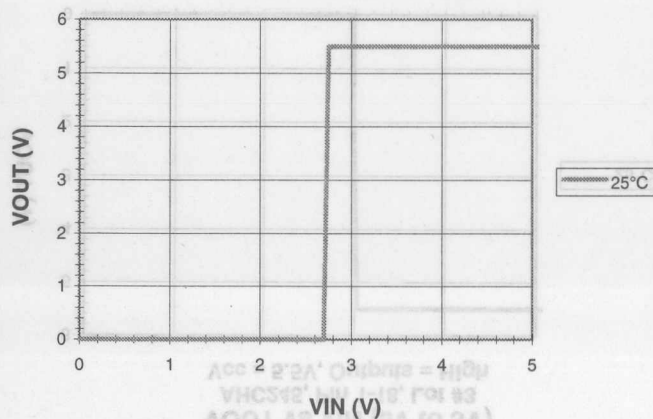
**VOUT vs VIN (0V to 5V)**  
**AHC245, Pin 1-18, Lot #3**  
**Vcc = 5.5V, Outputs = High**



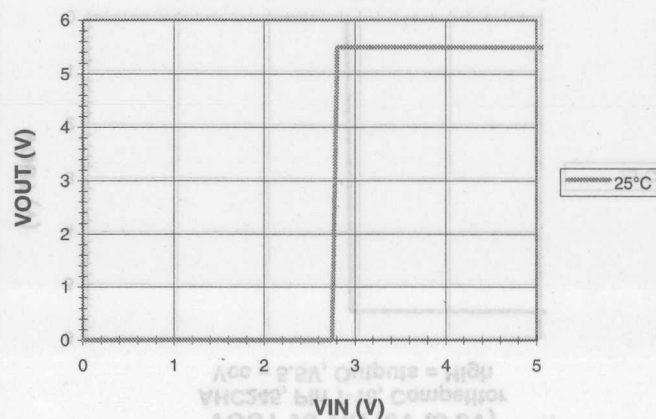
**VOUT vs VIN (0V to 5V)**  
**AHC245, Pin 1-18, Competitor**  
**Vcc = 5.5V, Outputs = High**



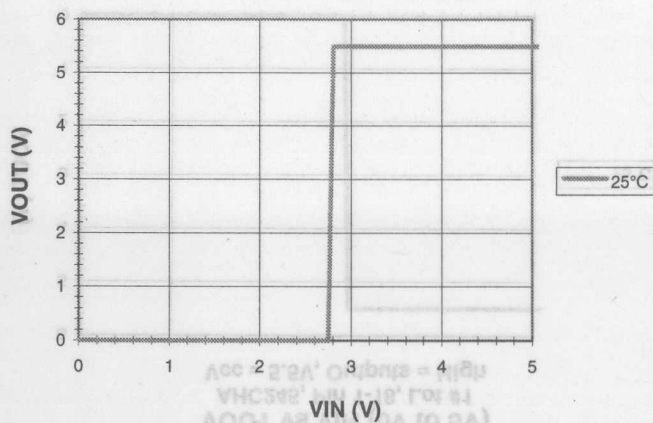
**VOUT vs VIN (5V to 0V)**  
AHC245, Pin 1-18, Lot #1  
Vcc = 5.5V, Outputs = High



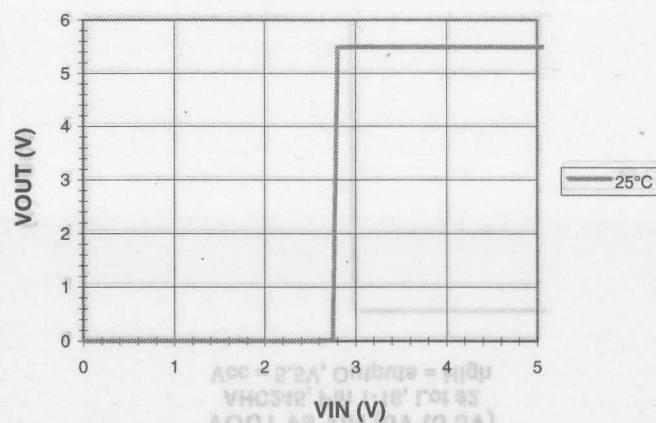
**VOUT vs VIN (5V to 0V)**  
AHC245, Pin 1-18, Lot #2  
Vcc = 5.5V, Outputs = High

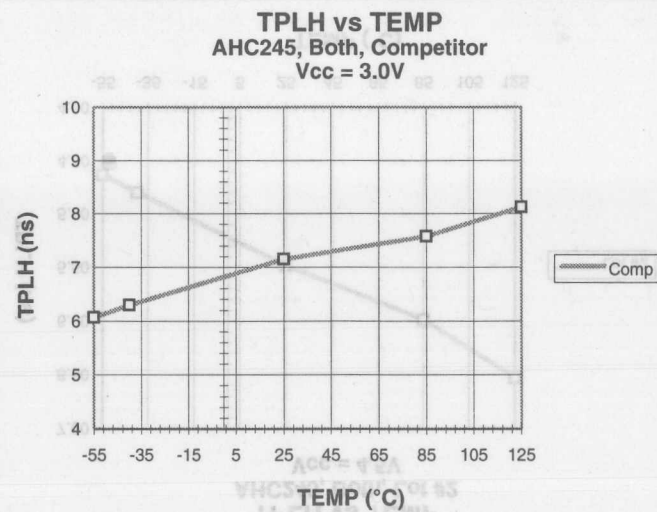
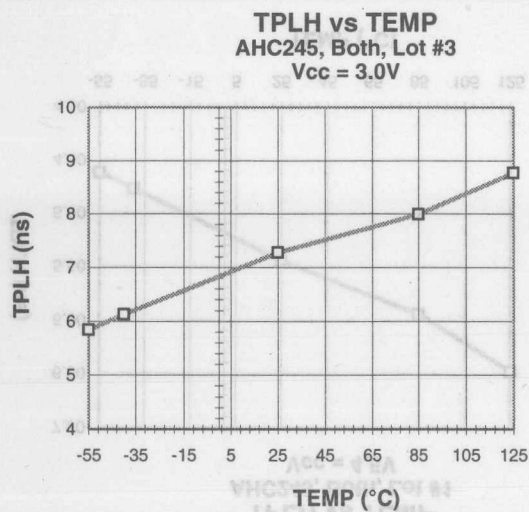
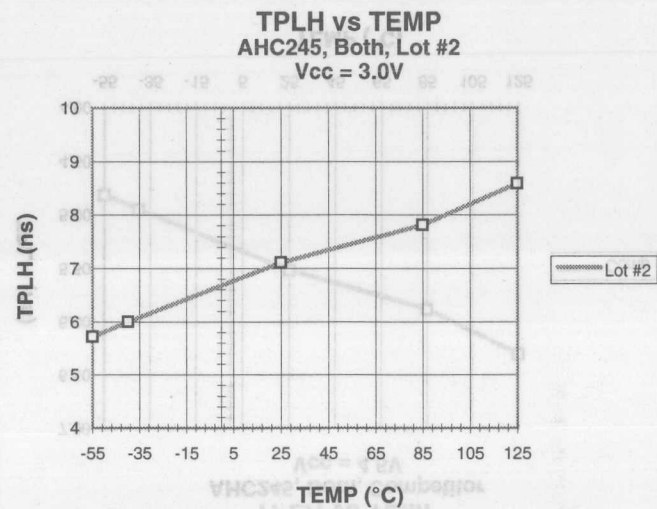
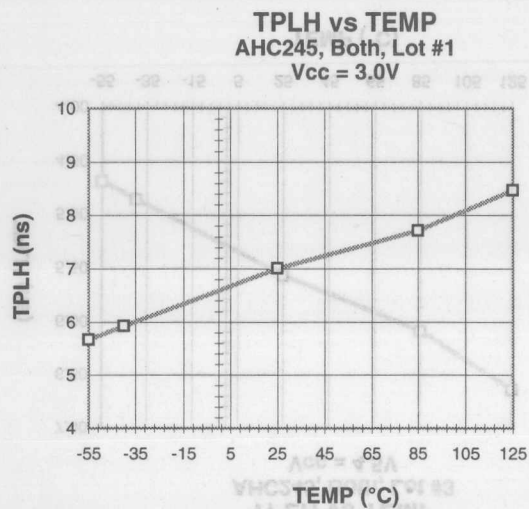


**VOUT vs VIN (5V to 0V)**  
AHC245, Pin 1-18, Lot #3  
Vcc = 5.5V, Outputs = High



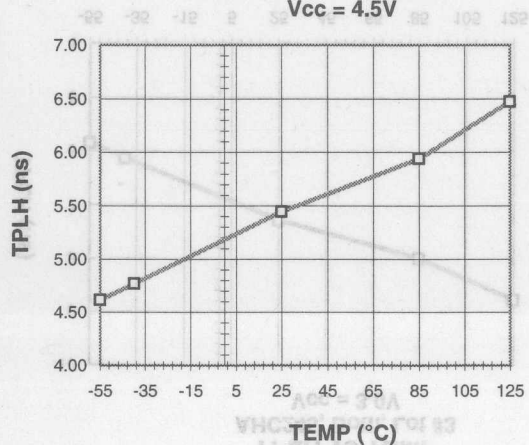
**VOUT vs VIN (5V to 0V)**  
AHC245, Pin 1-18, Competitor  
Vcc = 5.5V, Outputs = High





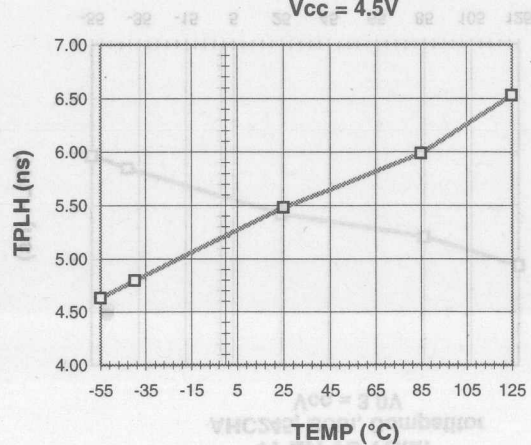


**TPLH vs TEMP**  
AHC245, Both, Lot #1  
Vcc = 4.5V



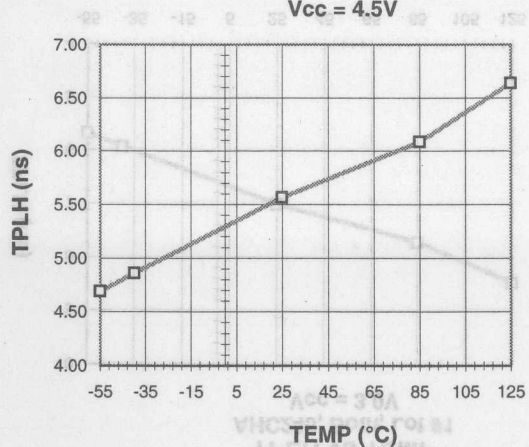
Lot #1

**TPLH vs TEMP**  
AHC245, Both, Lot #2  
Vcc = 4.5V



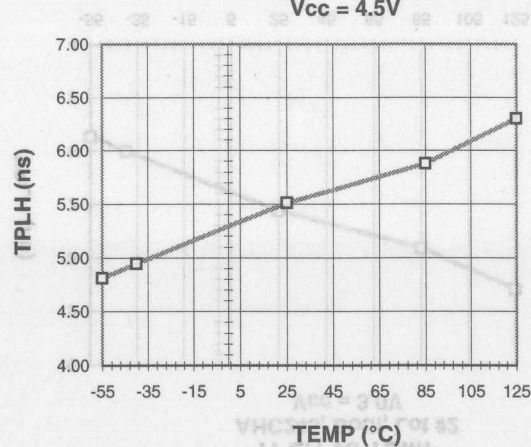
Lot #2

**TPLH vs TEMP**  
AHC245, Both, Lot #3  
Vcc = 4.5V



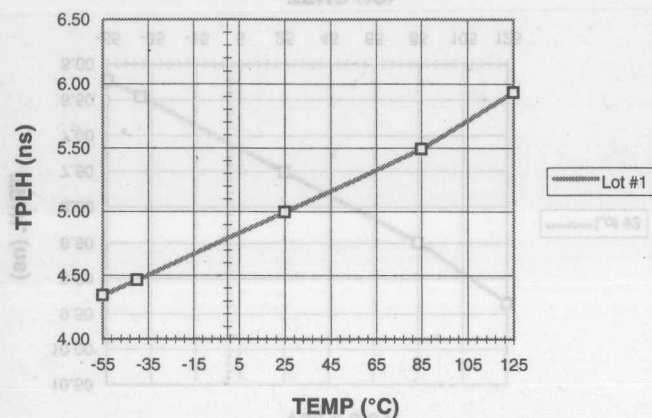
Lot #3

**TPLH vs TEMP**  
AHC245, Both, Competitor  
Vcc = 4.5V

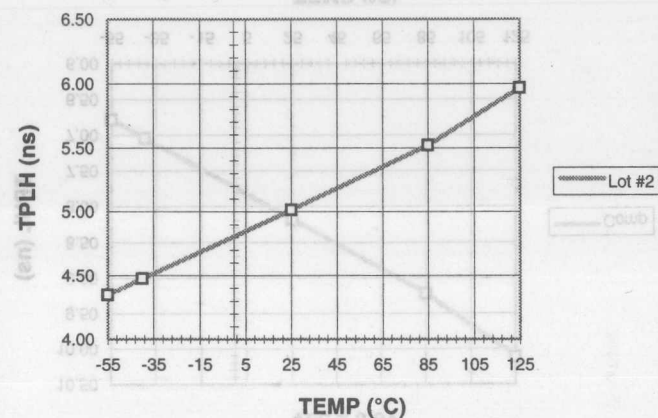


Comp

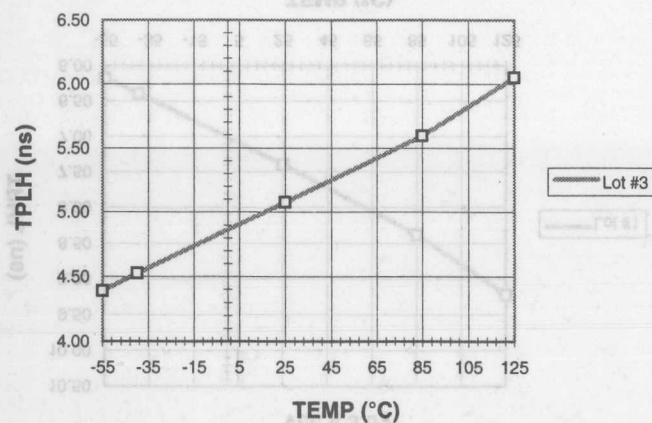
**TPLH vs TEMP**  
AHC245, Both, Lot #1  
Vcc = 5.5V



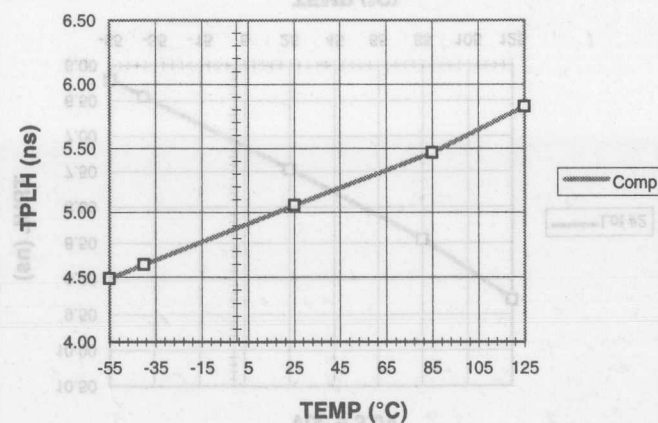
**TPLH vs TEMP**  
AHC245, Both, Lot #2  
Vcc = 5.5V



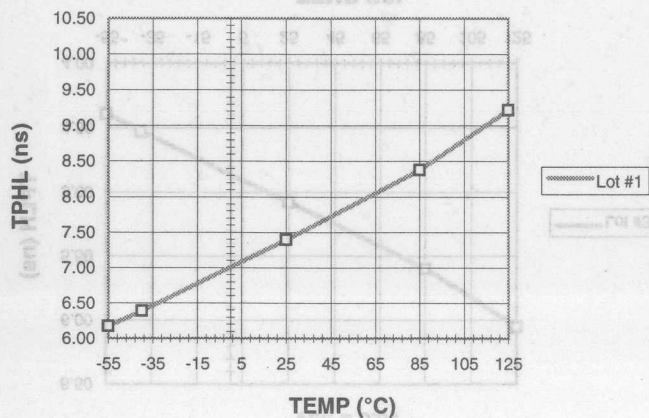
**TPLH vs TEMP**  
AHC245, Both, Lot #3  
Vcc = 5.5V



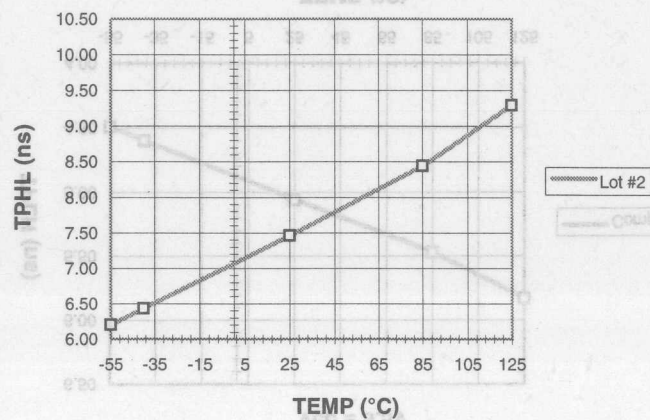
**TPLH vs TEMP**  
AHC245, Both, Competitor  
Vcc = 5.5V



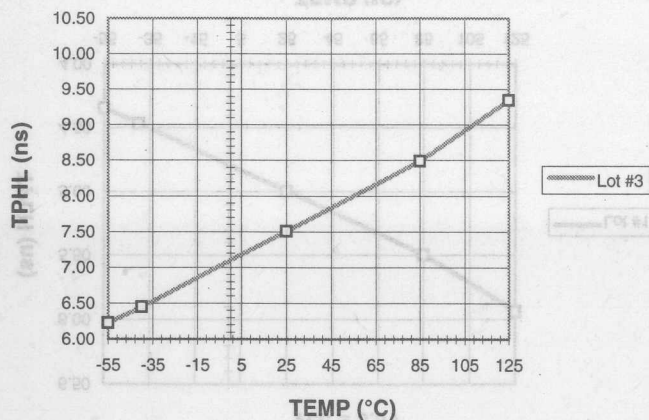
**TPHL vs TEMP**  
AHC245, Both, Lot #1  
Vcc = 3.0V



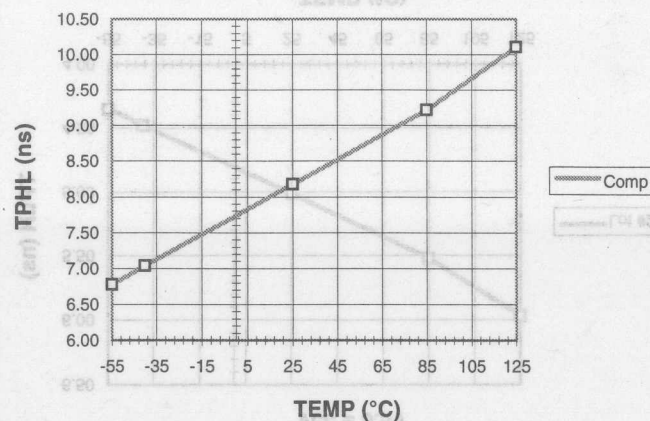
**TPHL vs TEMP**  
AHC245, Both, Lot #2  
Vcc = 3.0V

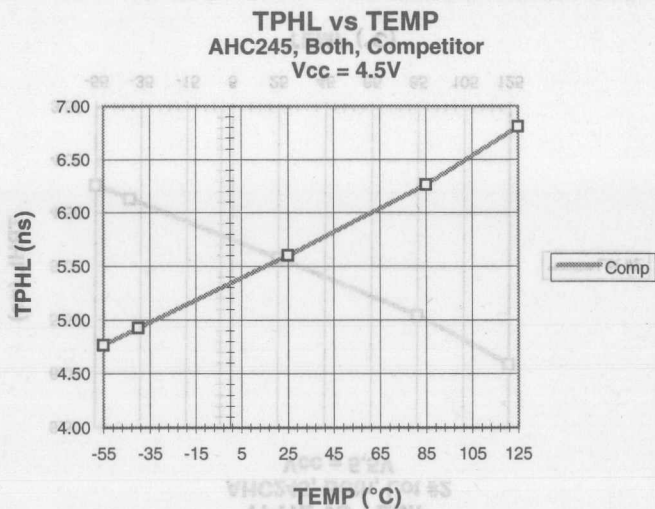
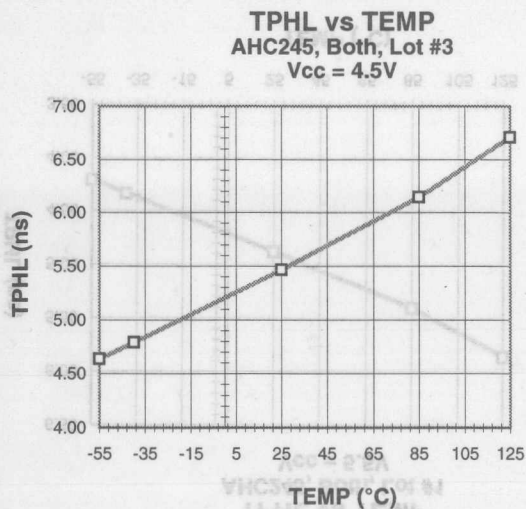
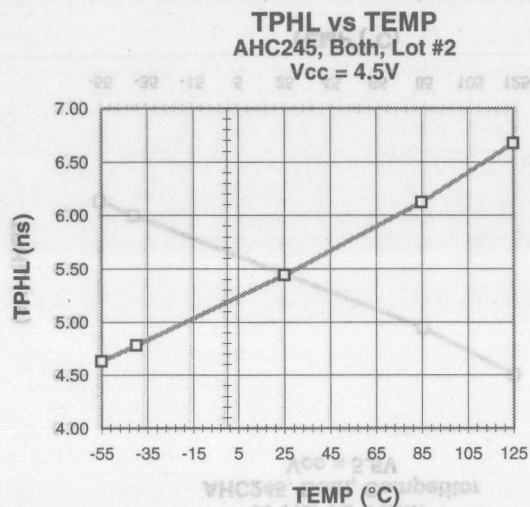
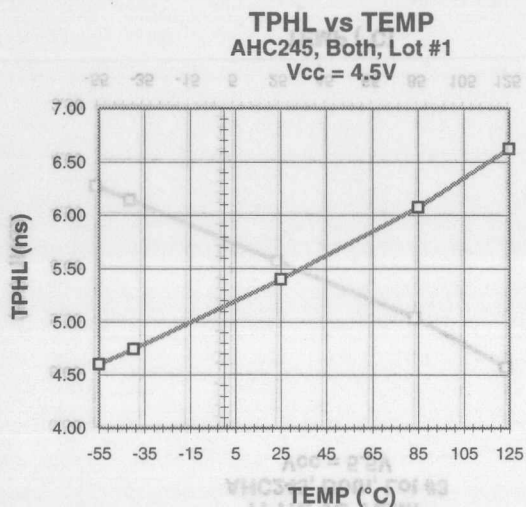


**TPHL vs TEMP**  
AHC245, Both, Lot #3  
Vcc = 3.0V

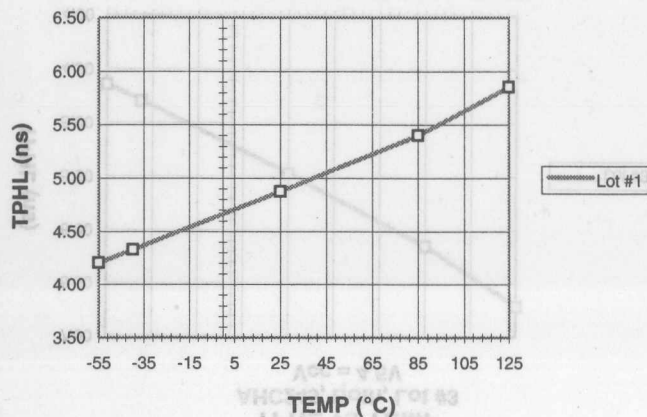


**TPHL vs TEMP**  
AHC245, Both, Competitor  
Vcc = 3.0V

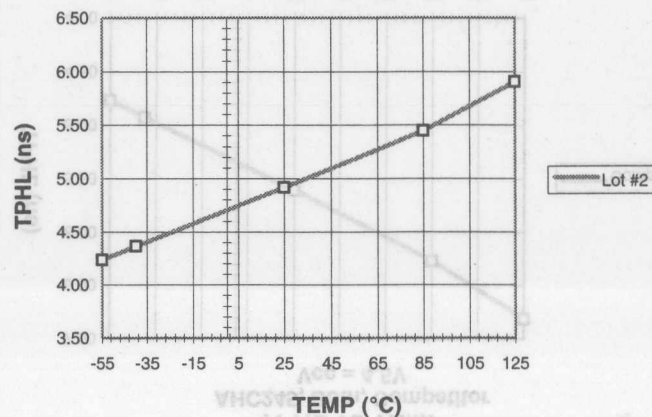




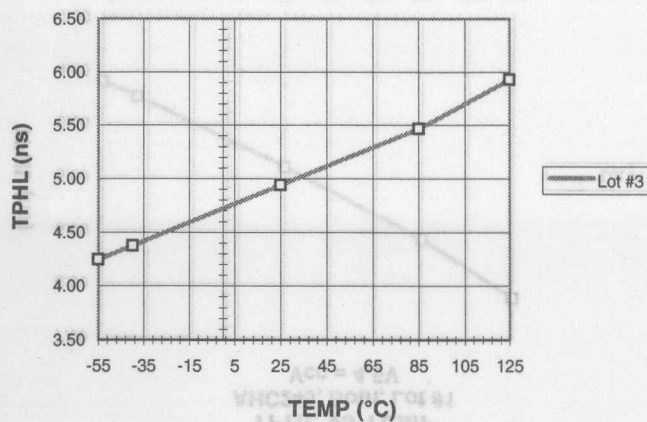
**TPHL vs TEMP**  
AHC245, Both, Lot #1  
Vcc = 5.5V



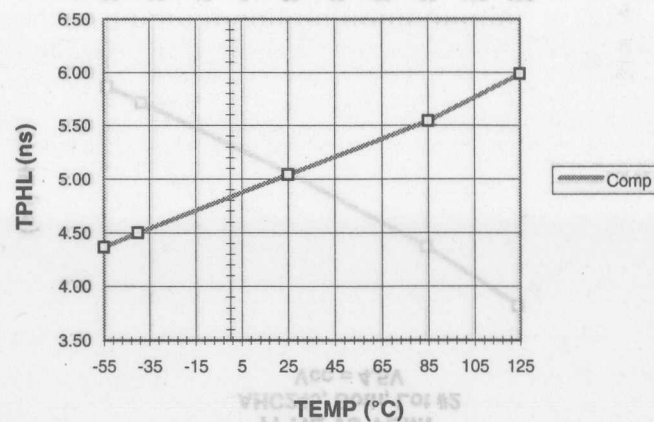
**TPHL vs TEMP**  
AHC245, Both, Lot #2  
Vcc = 5.5V



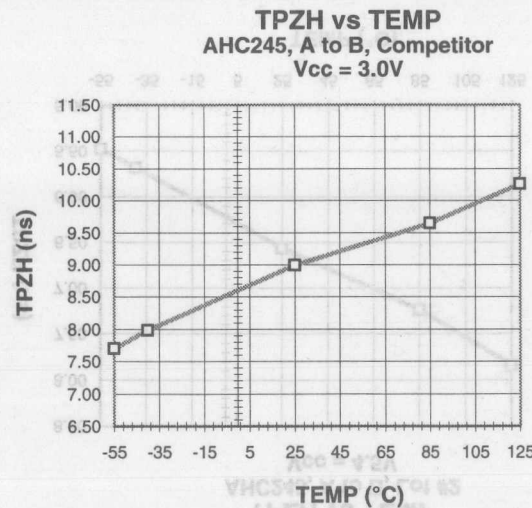
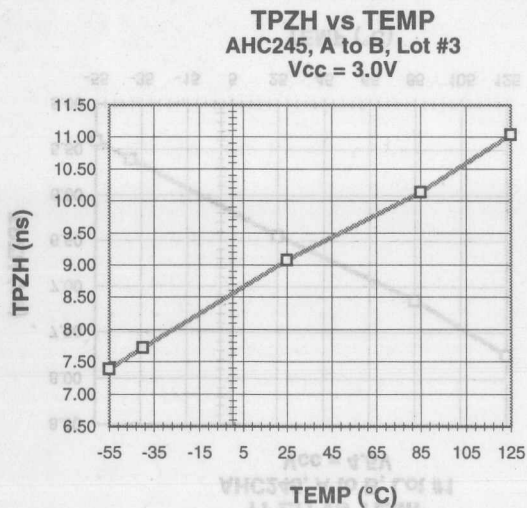
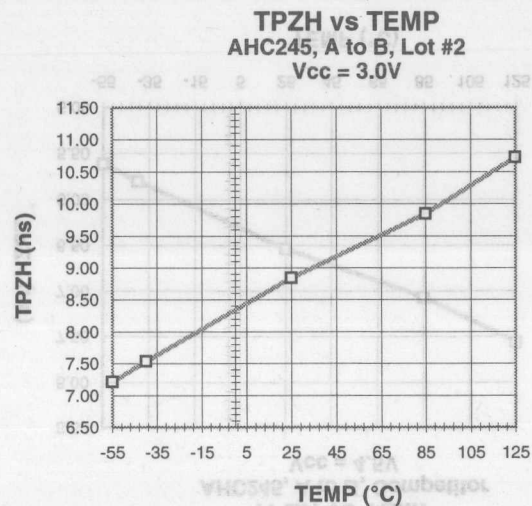
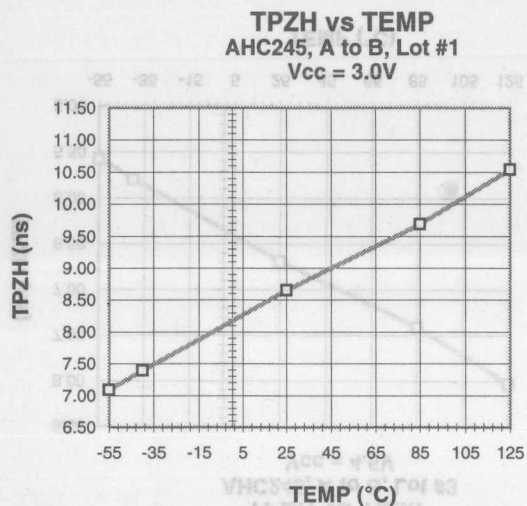
**TPHL vs TEMP**  
AHC245, Both, Lot #3  
Vcc = 5.5V



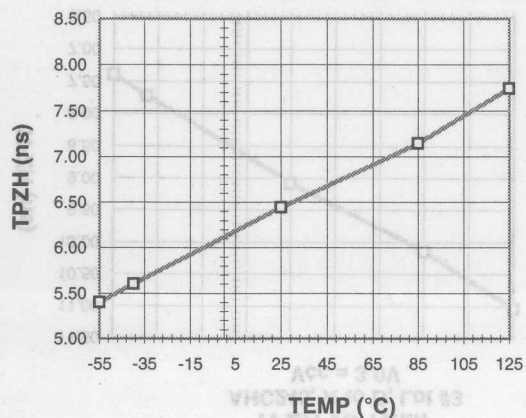
**TPHL vs TEMP**  
AHC245, Both, Competitor  
Vcc = 5.5V



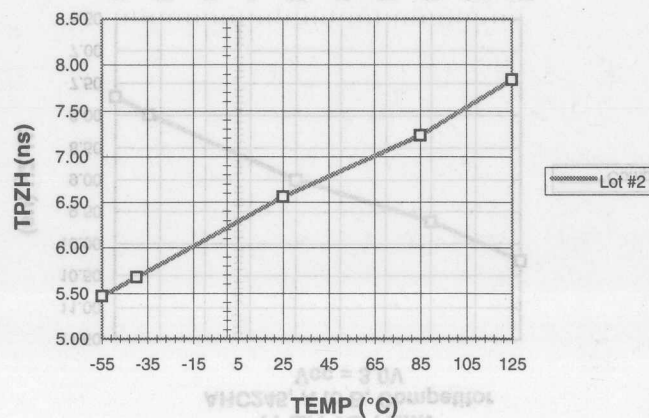




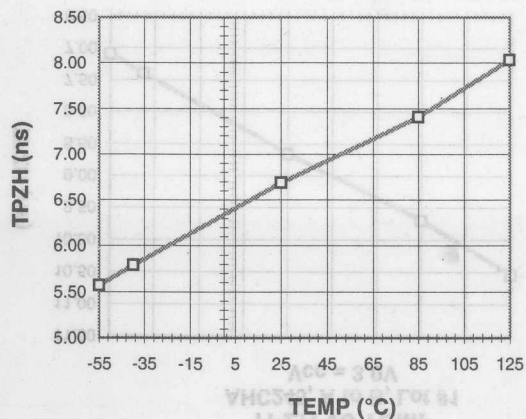
**TPZH vs TEMP**  
**AHC245, A to B, Lot #1**  
**Vcc = 4.5V**



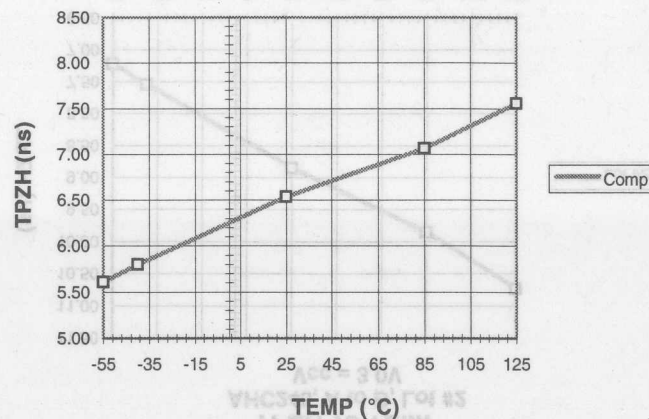
**TPZH vs TEMP**  
**AHC245, A to B, Lot #2**  
**Vcc = 4.5V**

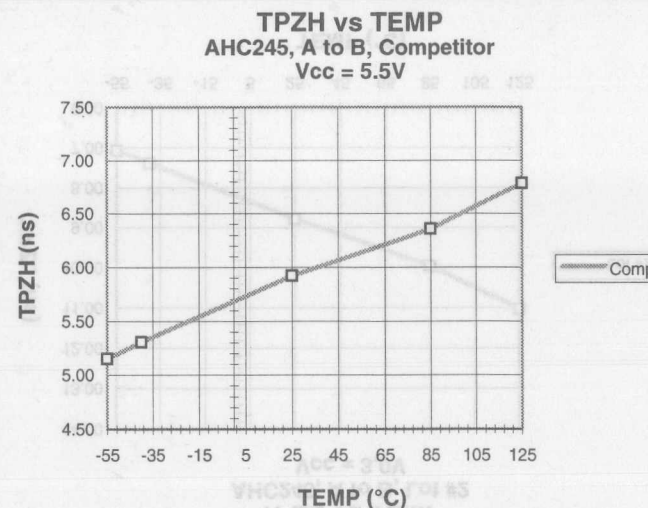
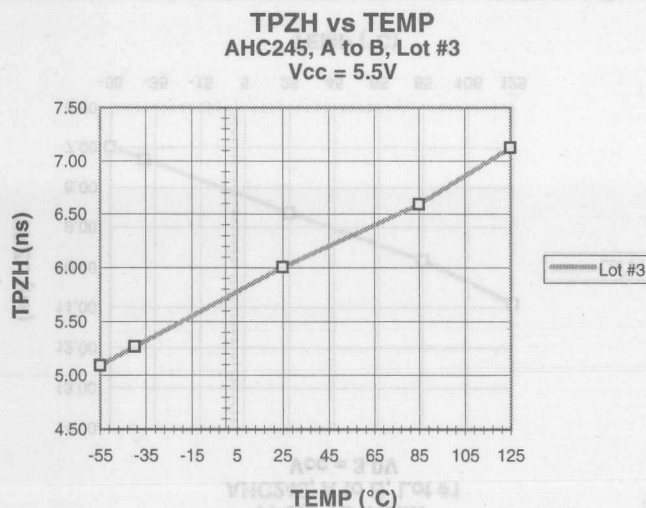
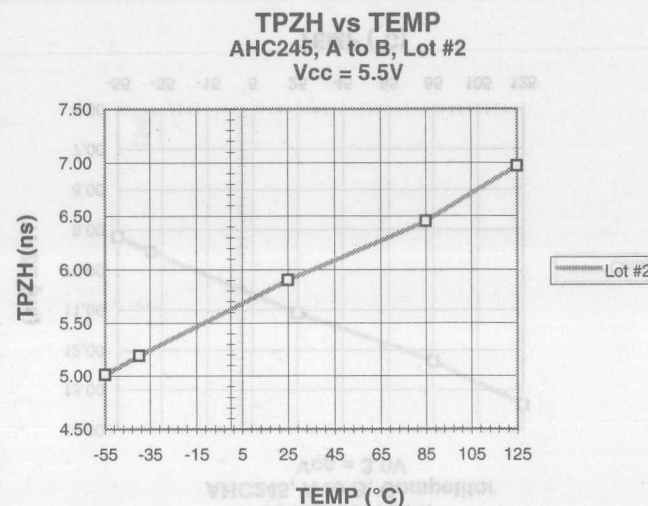
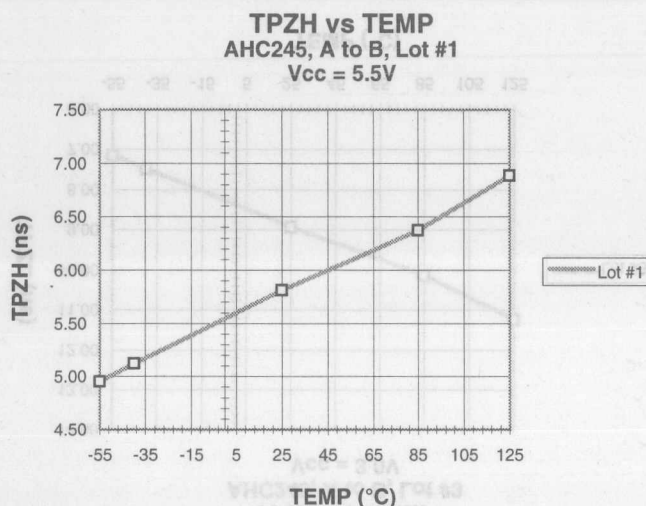


**TPZH vs TEMP**  
**AHC245, A to B, Lot #3**  
**Vcc = 4.5V**

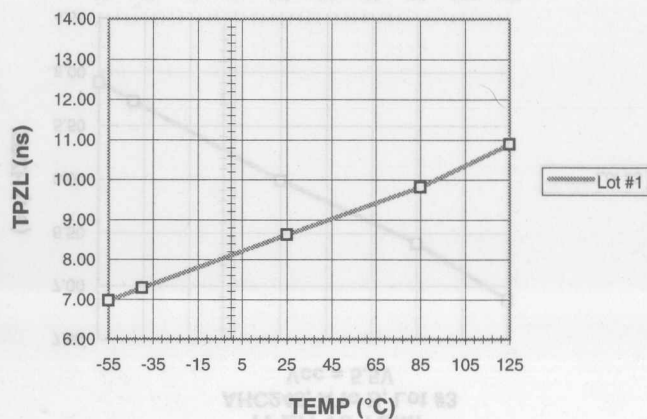


**TPZH vs TEMP**  
**AHC245, A to B, Competitor**  
**Vcc = 4.5V**

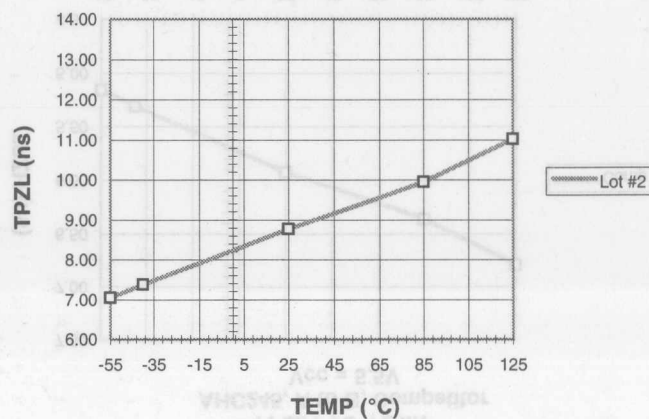




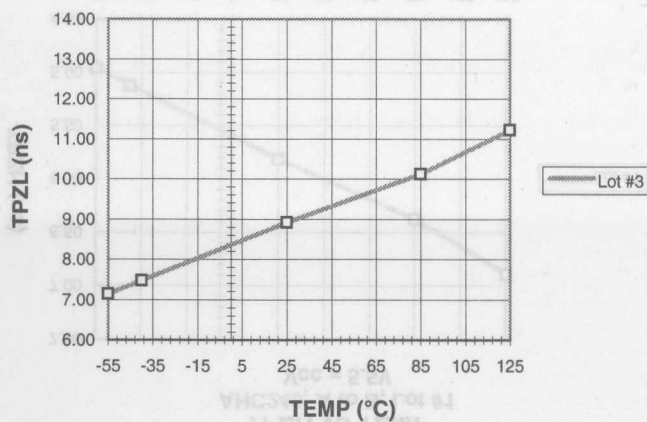
**TPZL vs TEMP**  
AHC245, A to B, Lot #1  
Vcc = 3.0V



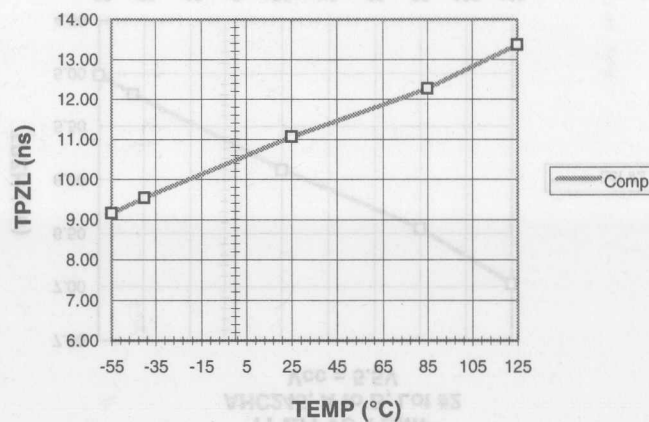
**TPZL vs TEMP**  
AHC245, A to B, Lot #2  
Vcc = 3.0V



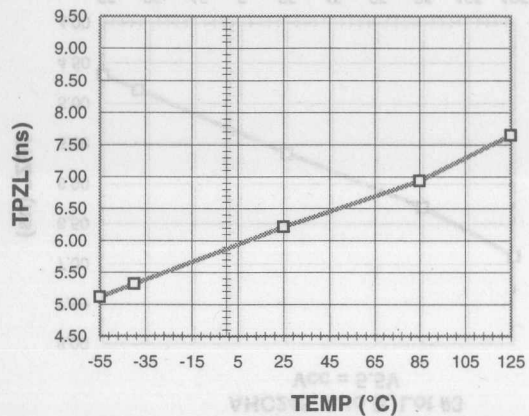
**TPZL vs TEMP**  
AHC245, A to B, Lot #3  
Vcc = 3.0V



**TPZL vs TEMP**  
AHC245, A to B, Competitor  
Vcc = 3.0V

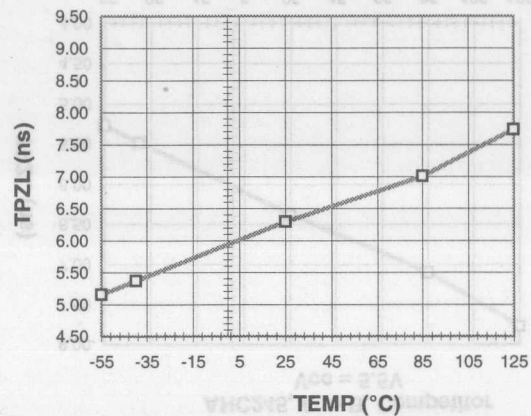


**TPZL vs TEMP**  
AHC245, A to B, Lot #1  
Vcc = 4.5V



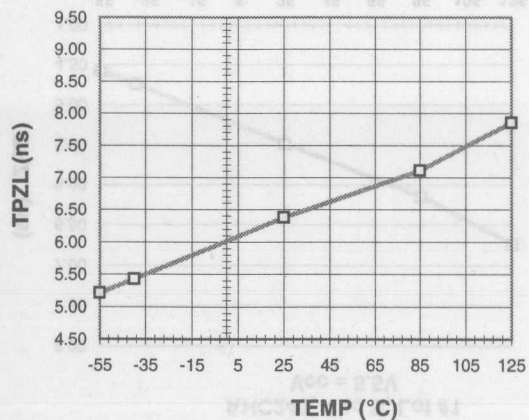
Lot #1

**TPZL vs TEMP**  
AHC245, A to B, Lot #2  
Vcc = 4.5V



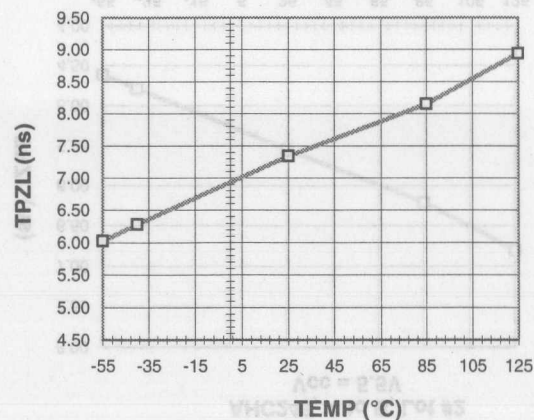
Lot #2

**TPZL vs TEMP**  
AHC245, A to B, Lot #3  
Vcc = 4.5V



Lot #3

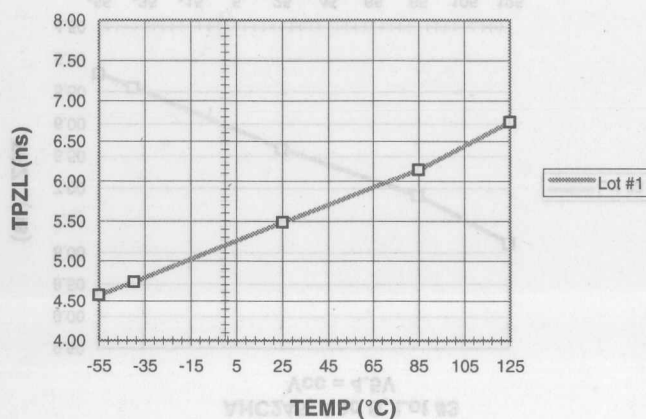
**TPZL vs TEMP**  
AHC245, A to B, Competitor  
Vcc = 4.5V



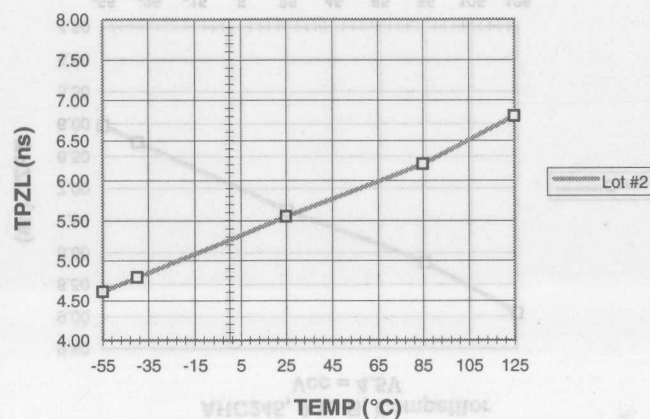
Comp



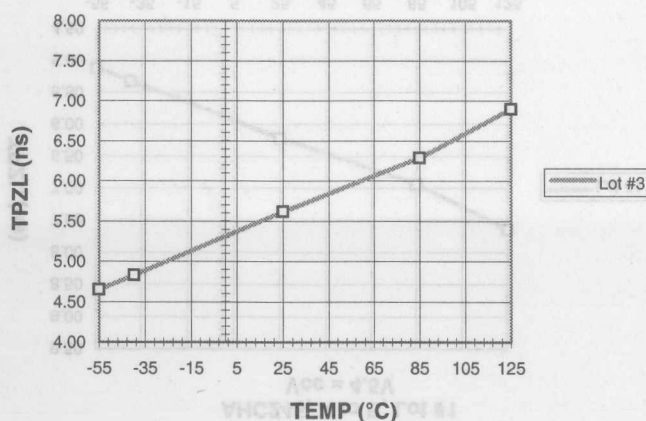
**TPZL vs TEMP**  
AHC245, A to B, Lot #1  
Vcc = 5.5V



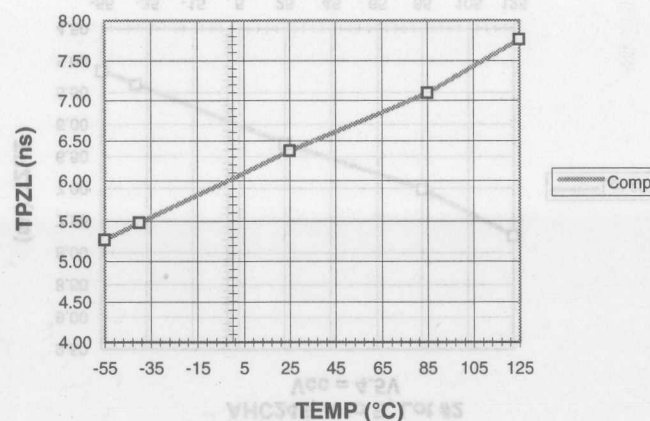
**TPZL vs TEMP**  
AHC245, A to B, Lot #2  
Vcc = 5.5V

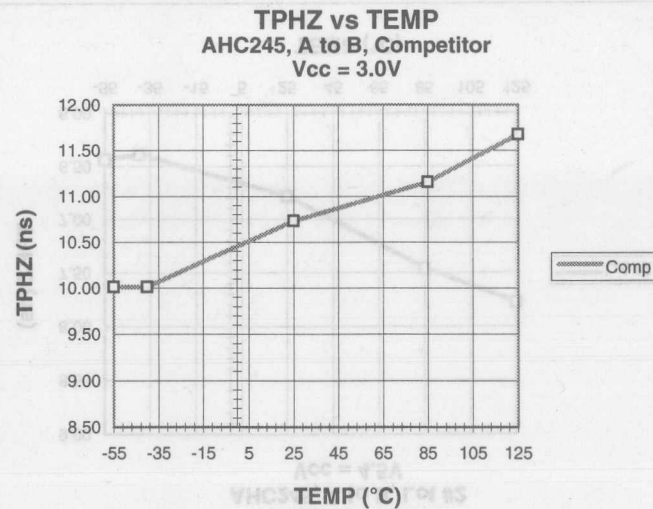
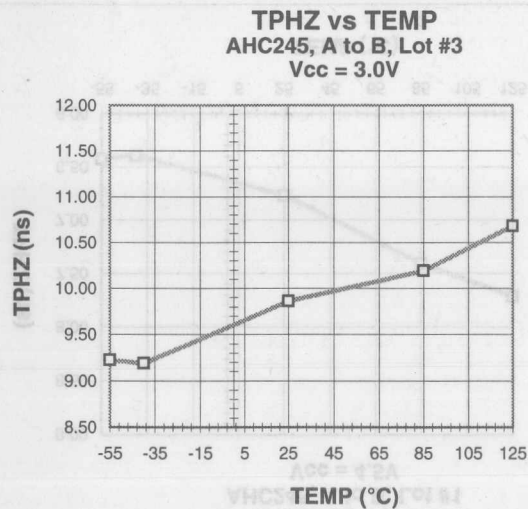
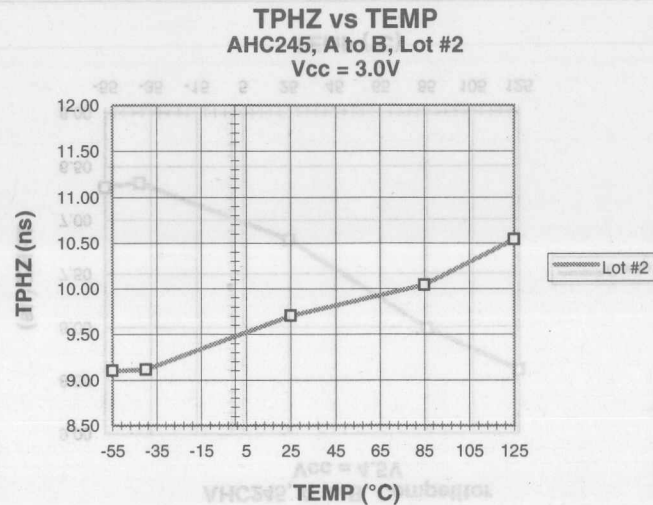
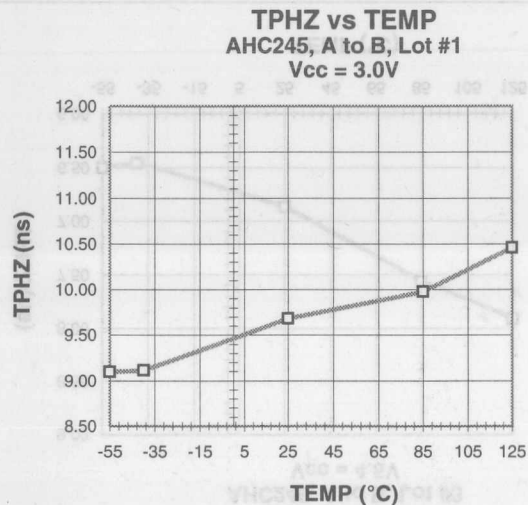


**TPZL vs TEMP**  
AHC245, A to B, Lot #3  
Vcc = 5.5V

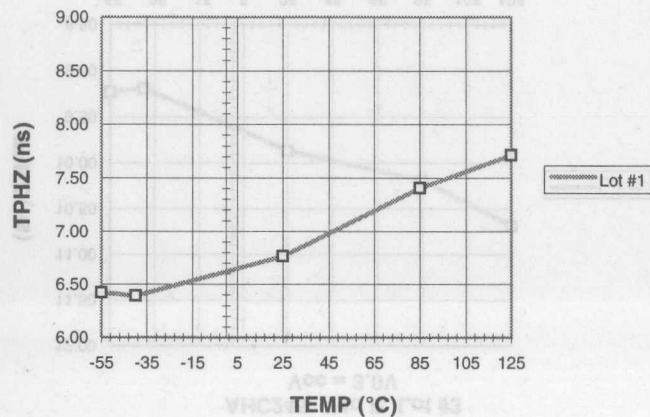


**TPZL vs TEMP**  
AHC245, A to B, Competitor  
Vcc = 5.5V

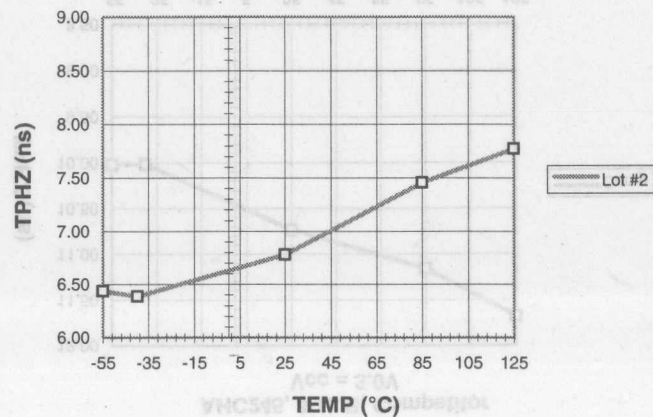




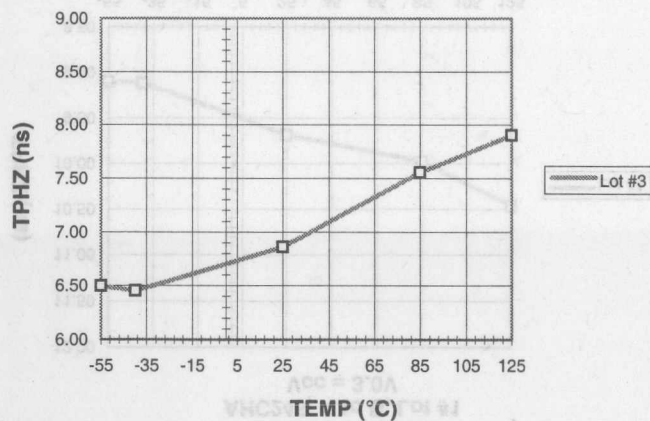
**TPHZ vs TEMP**  
AHC245, A to B, Lot #1  
Vcc = 4.5V



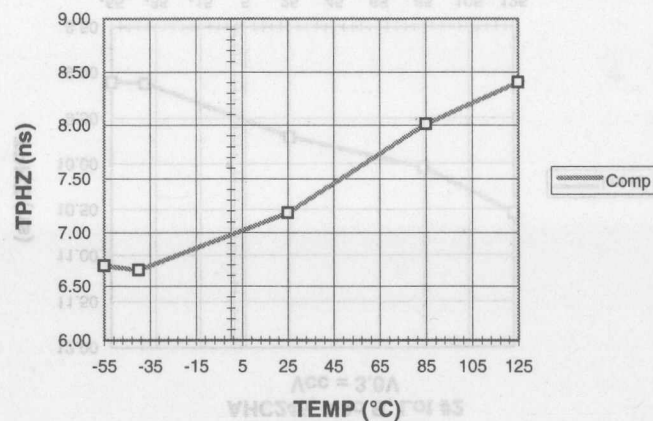
**TPHZ vs TEMP**  
AHC245, A to B, Lot #2  
Vcc = 4.5V

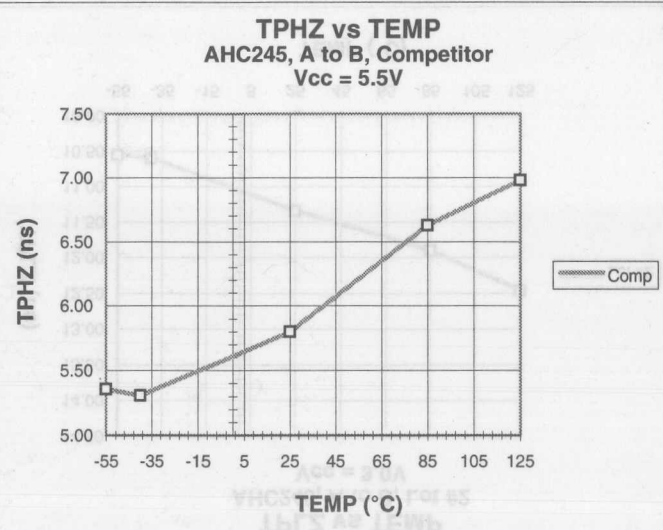
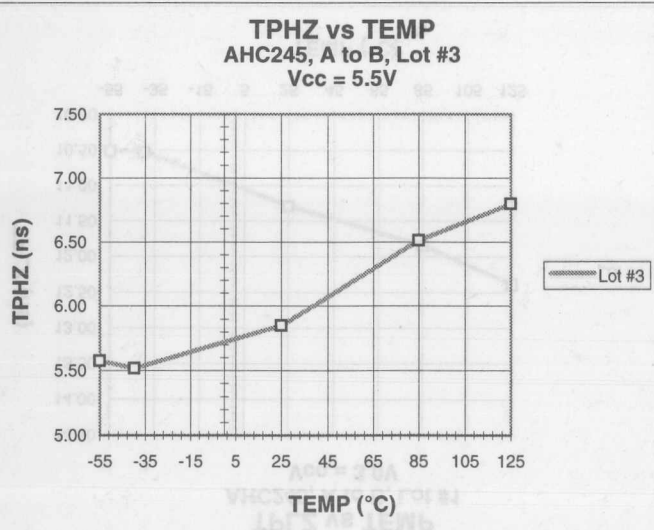
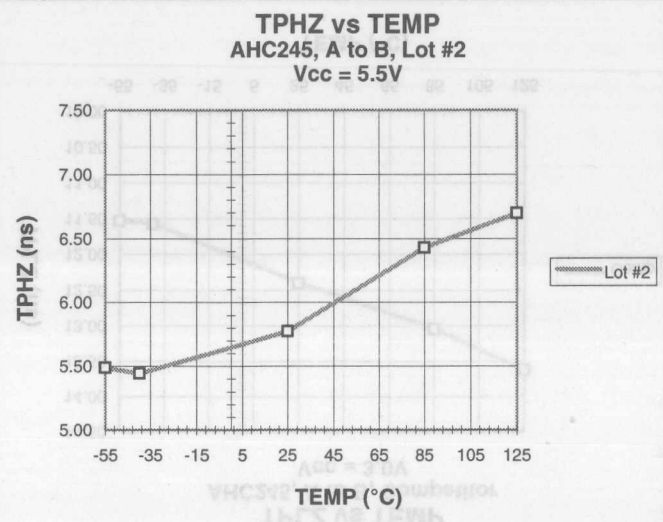
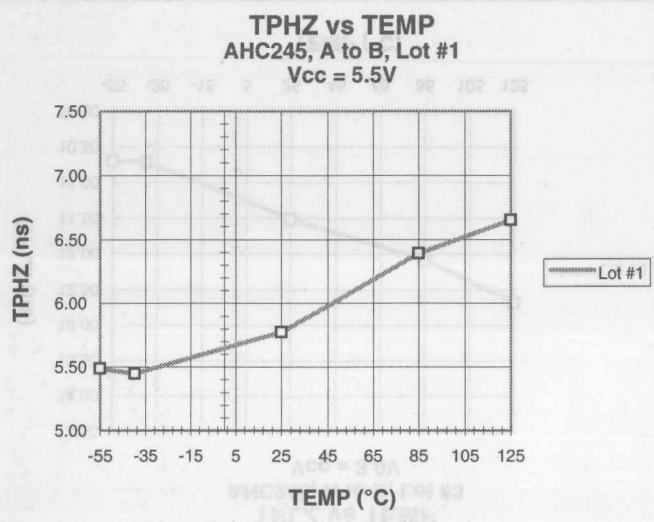


**TPHZ vs TEMP**  
AHC245, A to B, Lot #3  
Vcc = 4.5V

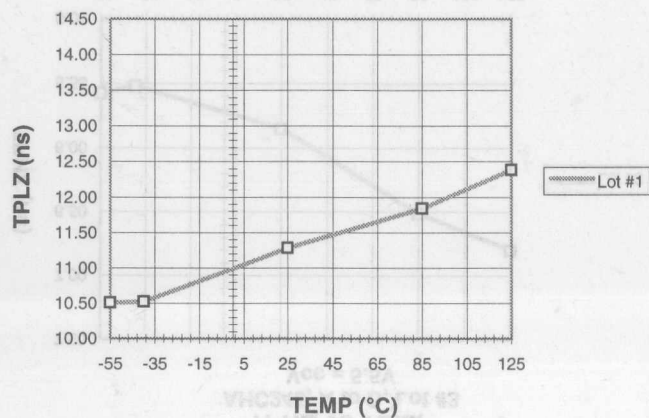


**TPHZ vs TEMP**  
AHC245, A to B, Competitor  
Vcc = 4.5V

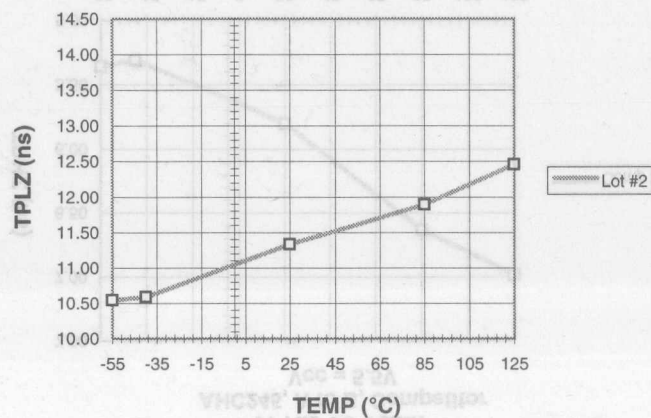




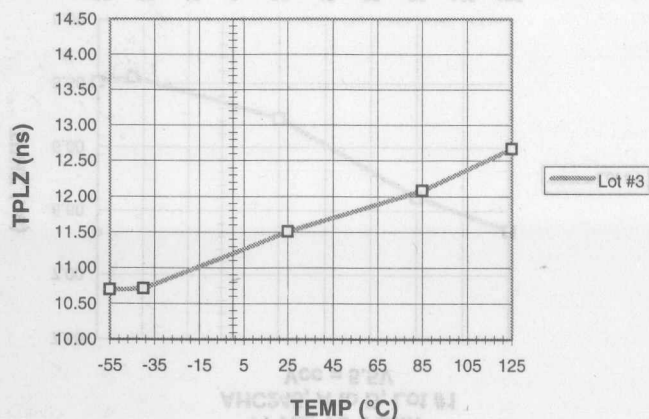
**TPLZ vs TEMP**  
AHC245, A to B, Lot #1  
Vcc = 3.0V



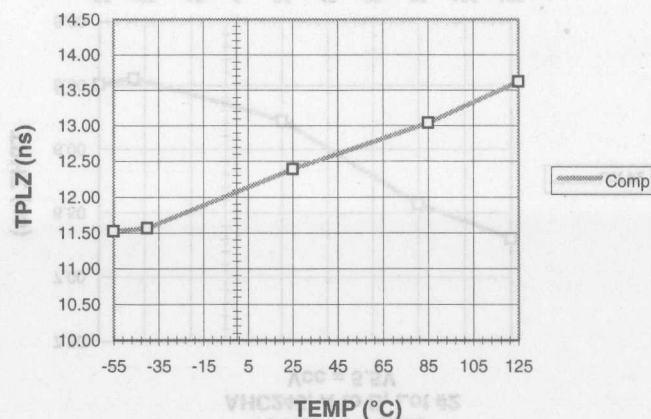
**TPLZ vs TEMP**  
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Vcc = 3.0V



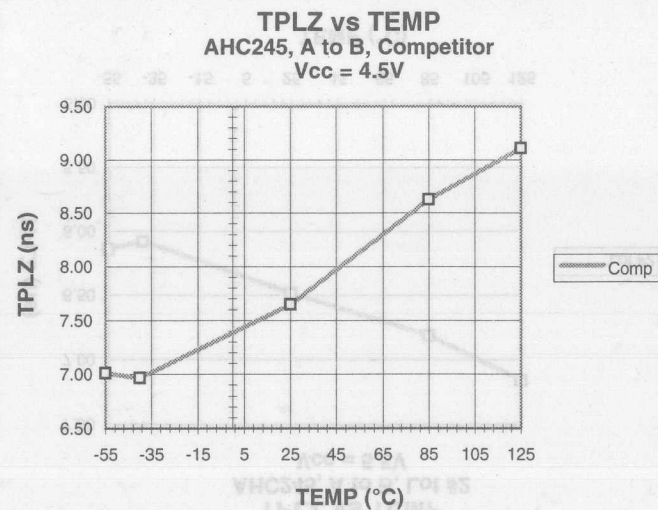
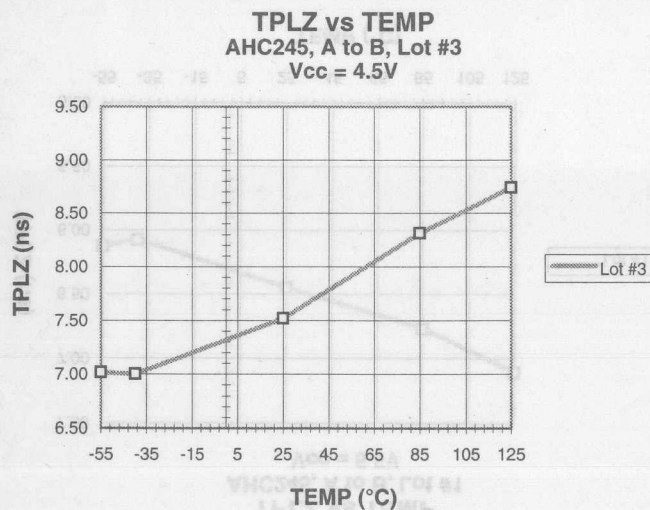
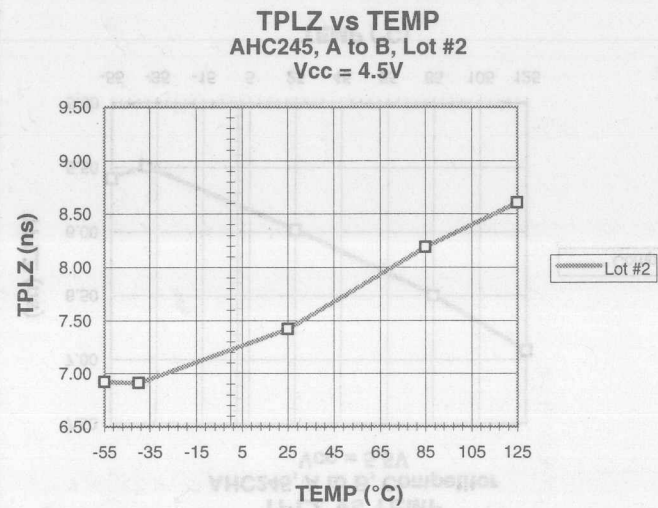
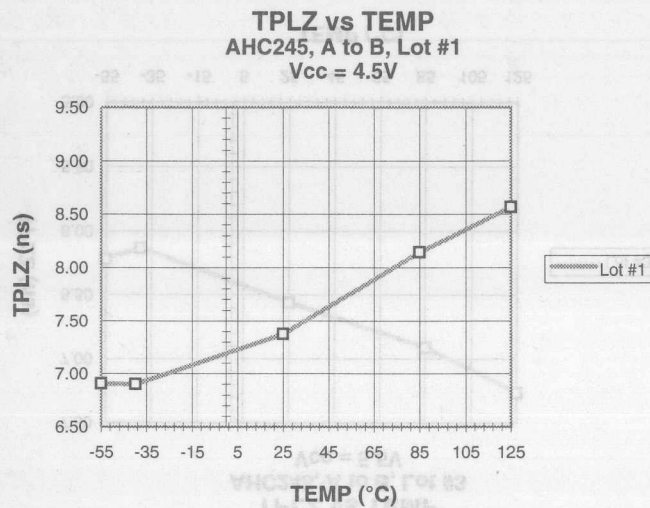
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AHC245, A to B, Lot #3  
Vcc = 3.0V



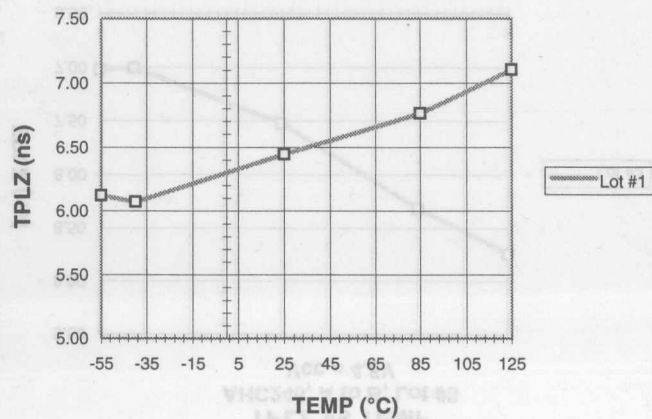
**TPLZ vs TEMP**  
AHC245, A to B, Competitor  
Vcc = 3.0V



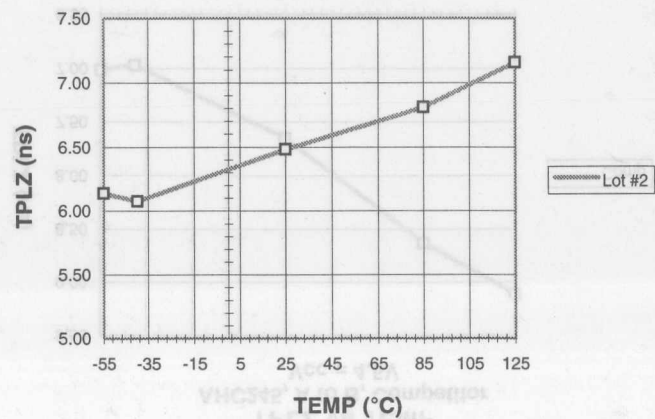




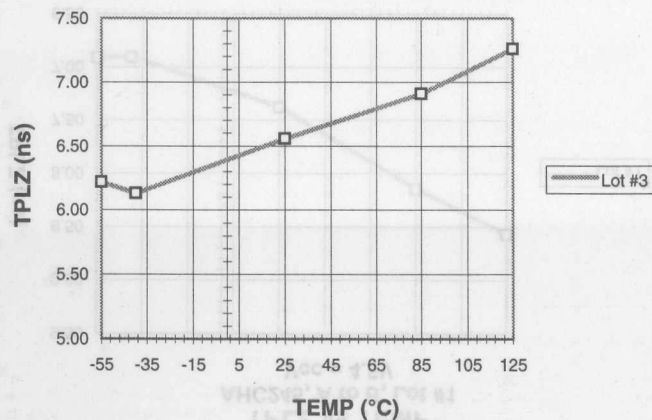
**TPLZ vs TEMP**  
AHC245, A to B, Lot #1  
Vcc = 5.5V



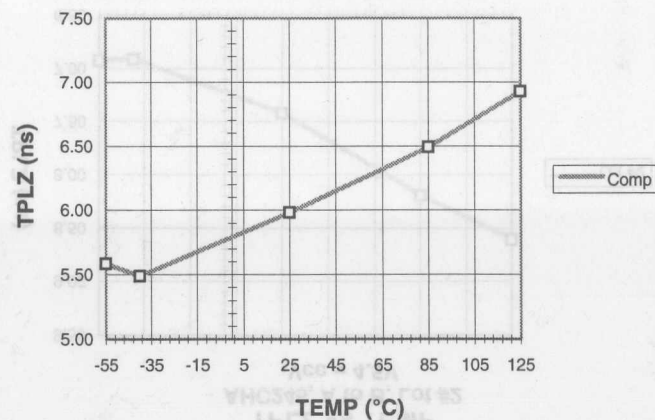
**TPLZ vs TEMP**  
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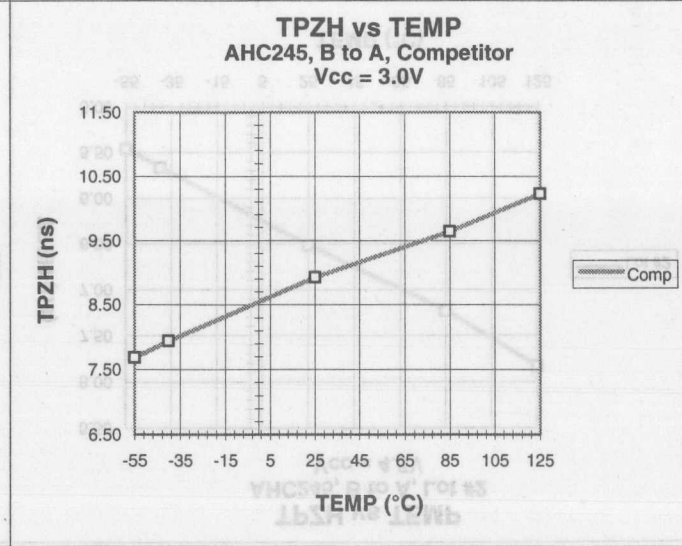
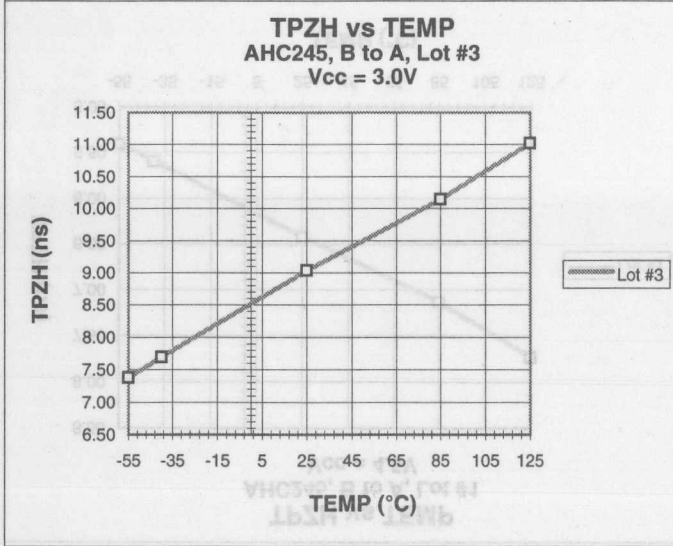
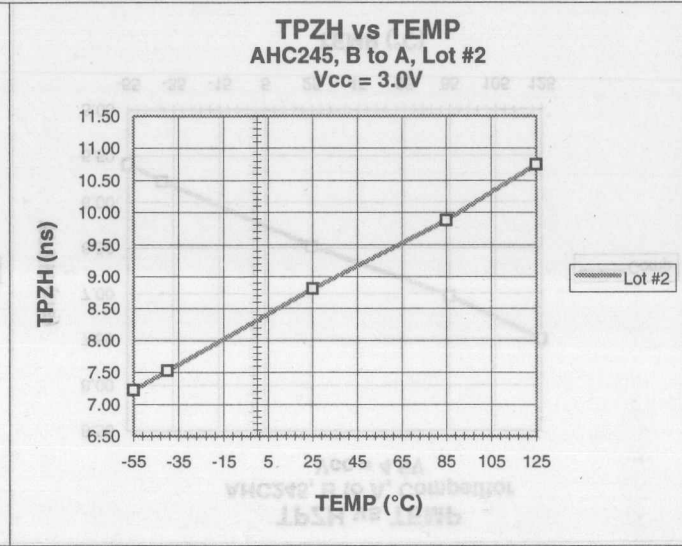
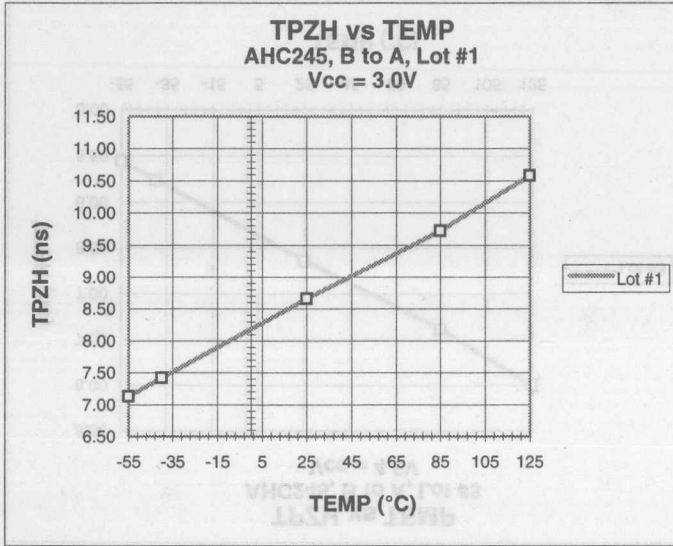


**TPLZ vs TEMP**  
AHC245, A to B, Lot #3  
Vcc = 5.5V

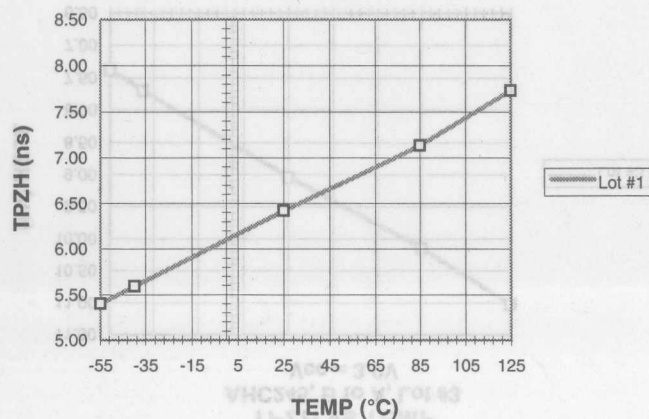


**TPLZ vs TEMP**  
AHC245, A to B, Competitor  
Vcc = 5.5V

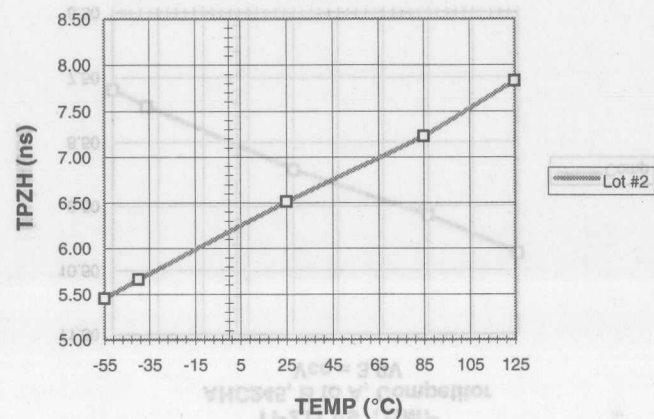




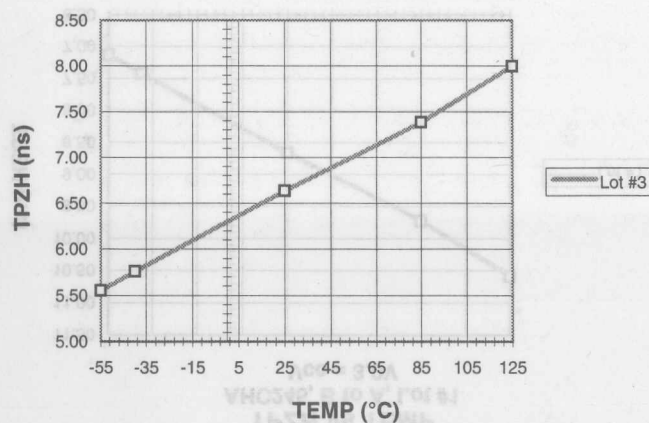
**TPZH vs TEMP**  
**AHC245, B to A, Lot #1**  
**Vcc = 4.5V**



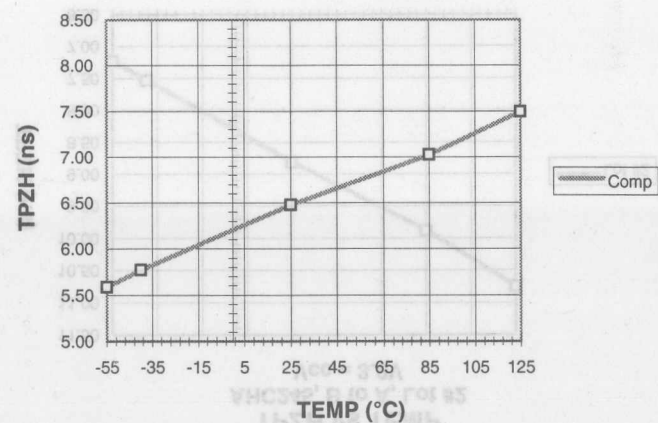
**TPZH vs TEMP**  
**AHC245, B to A, Lot #2**  
**Vcc = 4.5V**

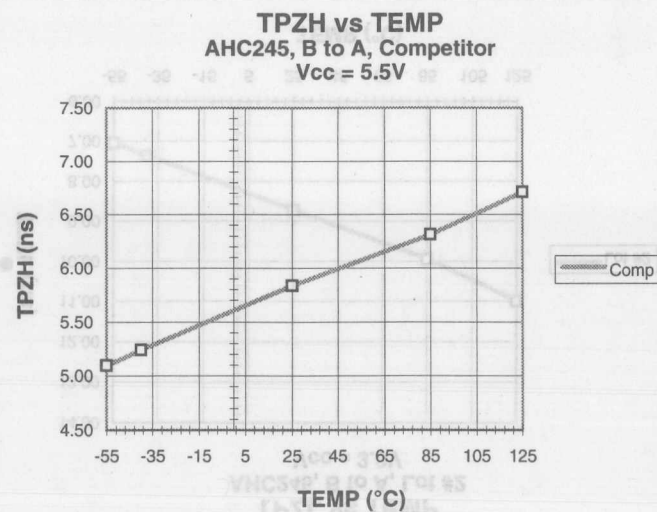
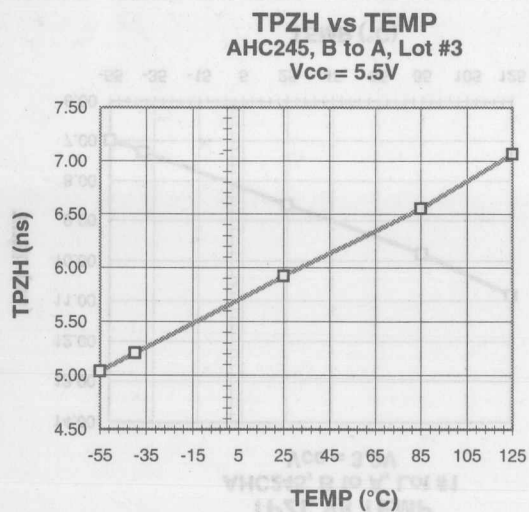
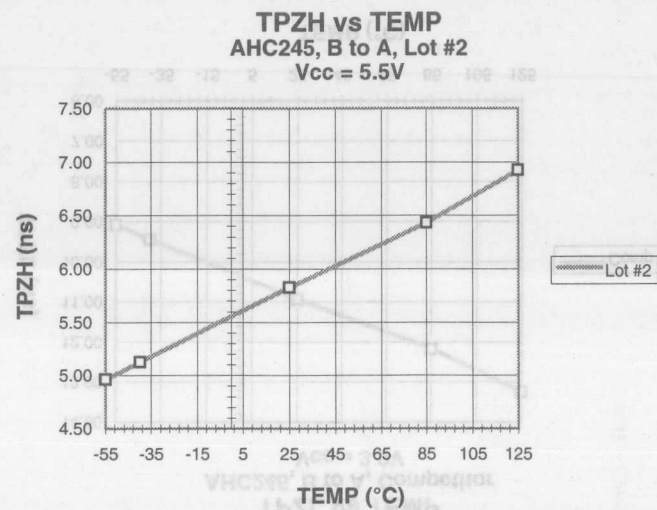
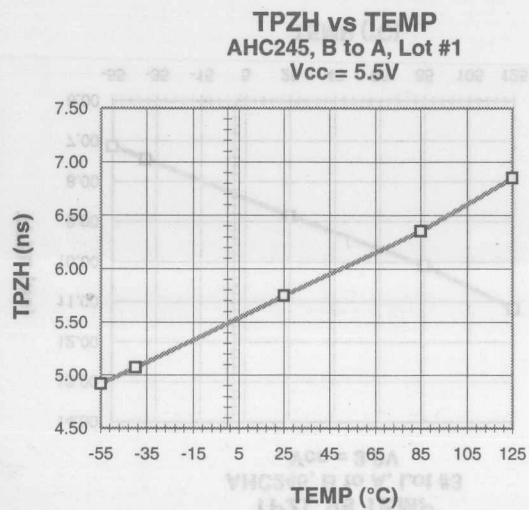


**TPZH vs TEMP**  
**AHC245, B to A, Lot #3**  
**Vcc = 4.5V**



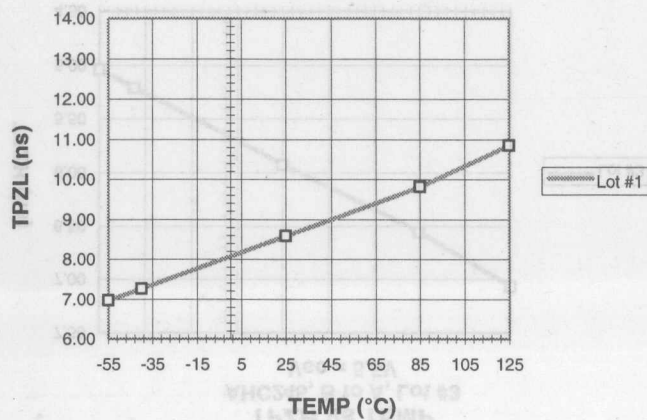
**TPZH vs TEMP**  
**AHC245, B to A, Competitor**  
**Vcc = 4.5V**



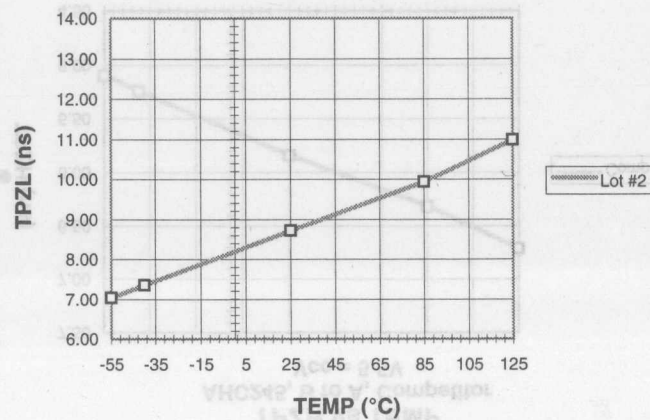




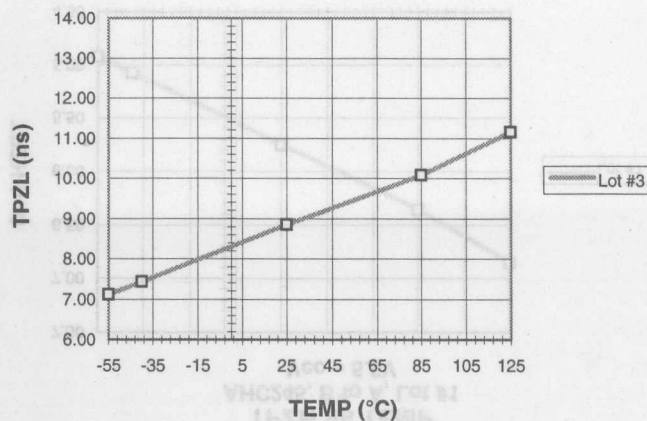
**TPZL vs TEMP**  
AHC245, B to A, Lot #1  
Vcc = 3.0V



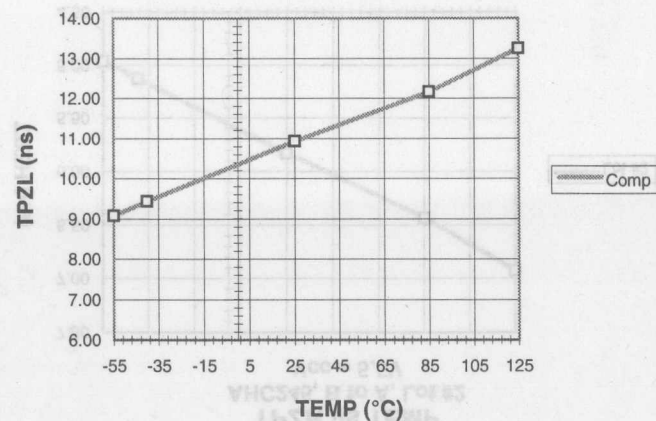
**TPZL vs TEMP**  
AHC245, B to A, Lot #2  
Vcc = 3.0V

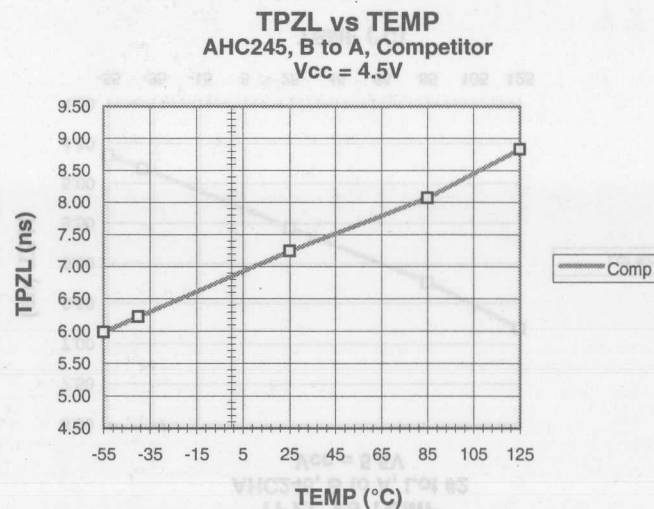
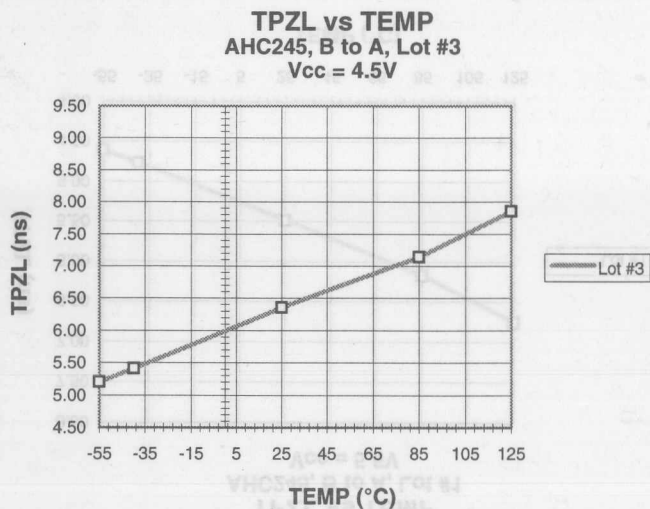
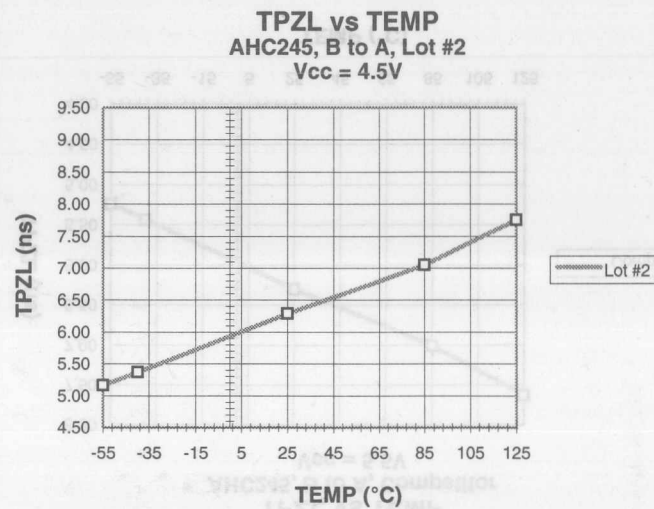
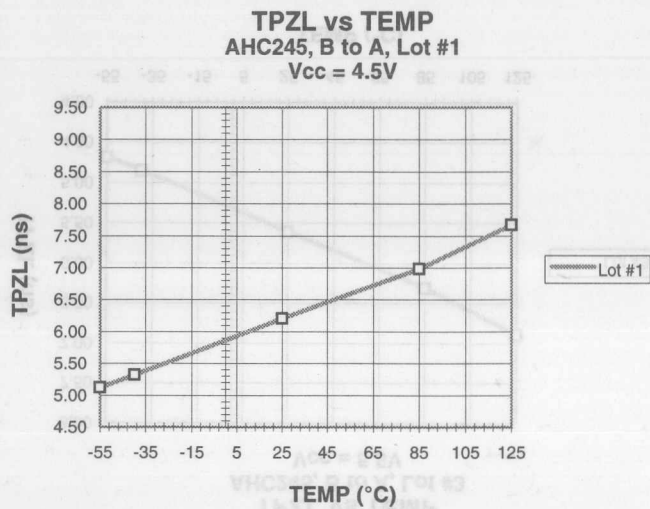


**TPZL vs TEMP**  
AHC245, B to A, Lot #3  
Vcc = 3.0V

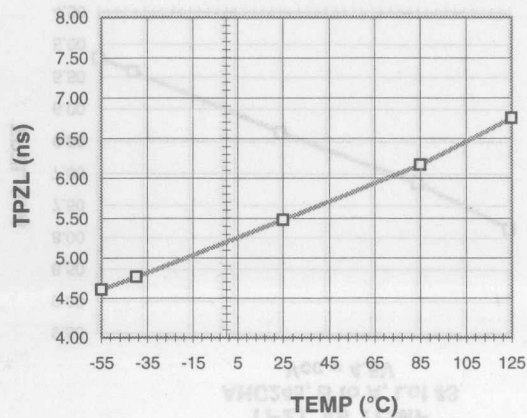


**TPZL vs TEMP**  
AHC245, B to A, Competitor  
Vcc = 3.0V

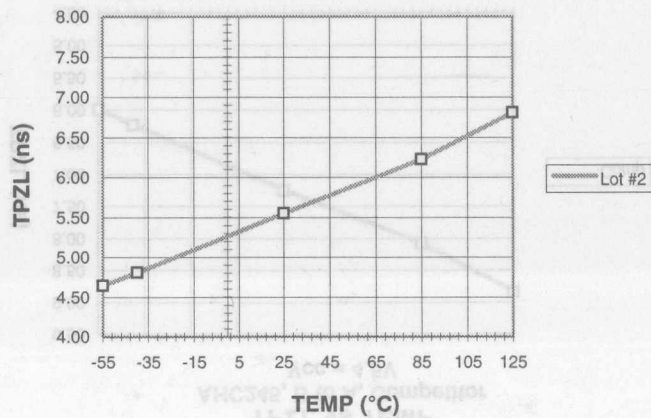




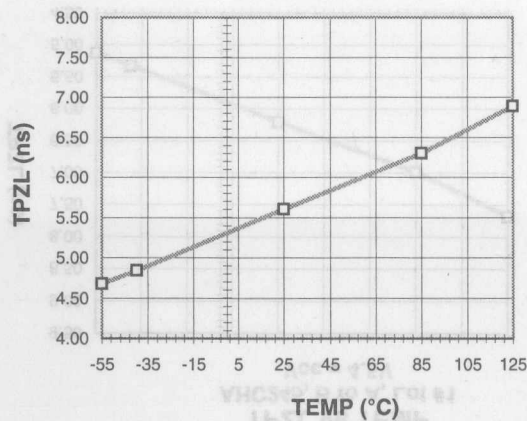
**TPZL vs TEMP**  
AHC245, B to A, Lot #1  
Vcc = 5.5V



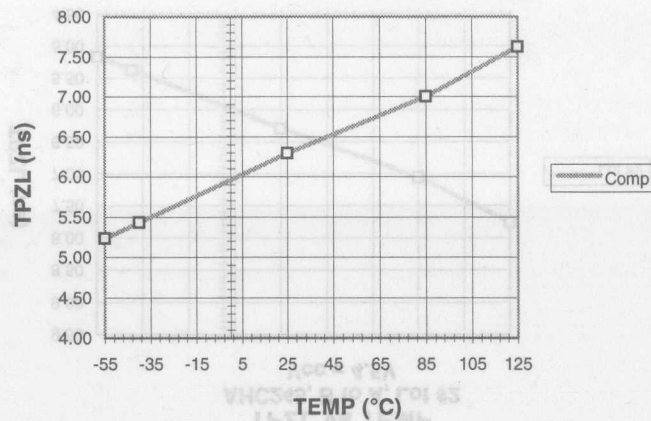
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AHC245, B to A, Lot #2  
Vcc = 5.5V

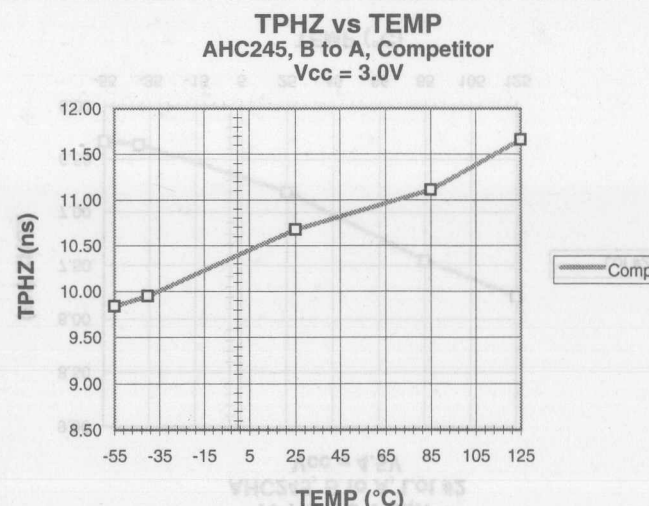
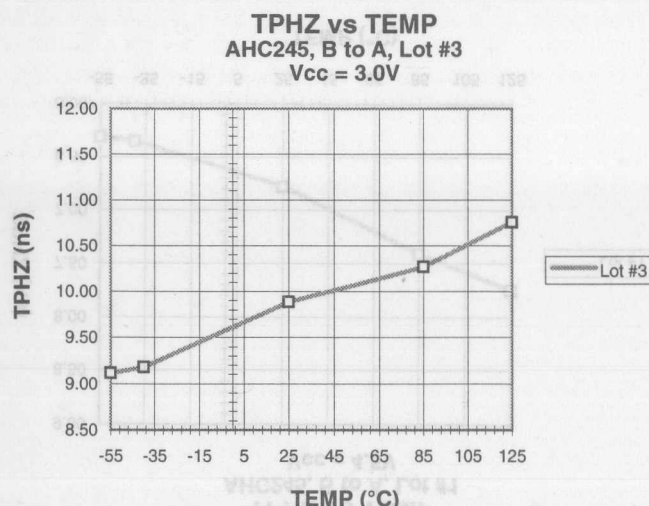
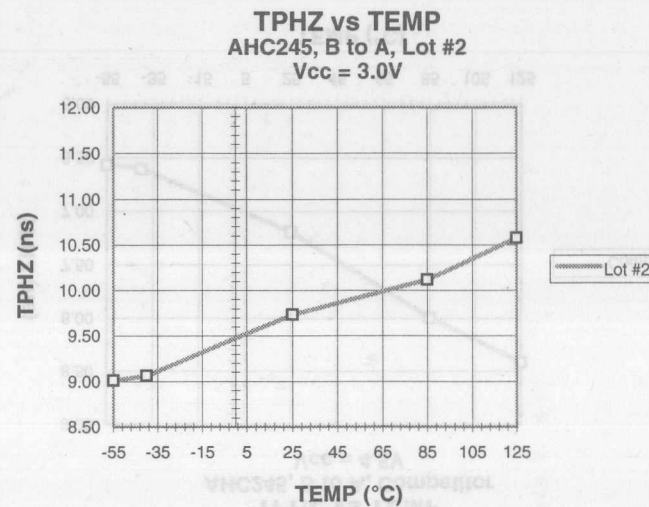
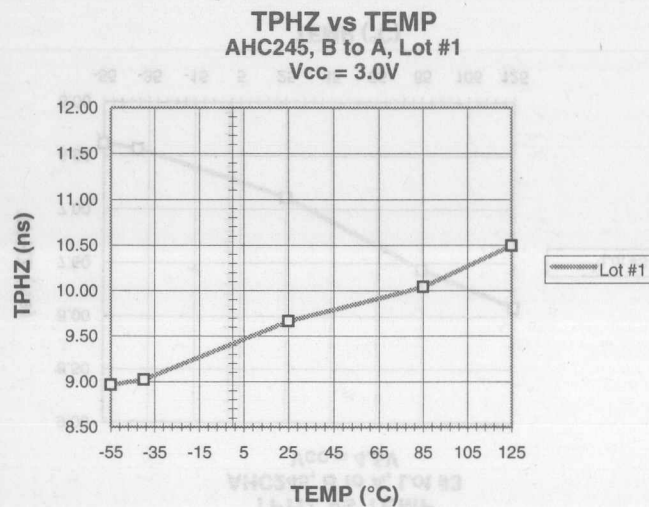


**TPZL vs TEMP**  
AHC245, B to A, Lot #3  
Vcc = 5.5V

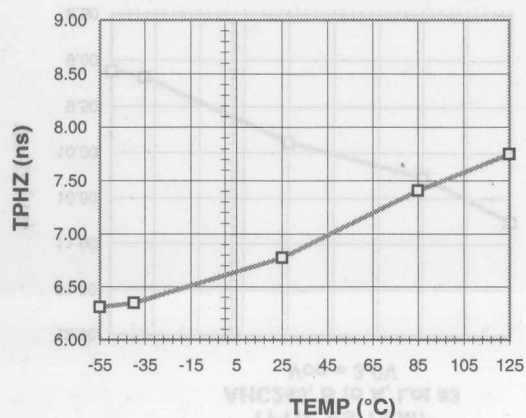


**TPZL vs TEMP**  
AHC245, B to A, Competitor  
Vcc = 5.5V

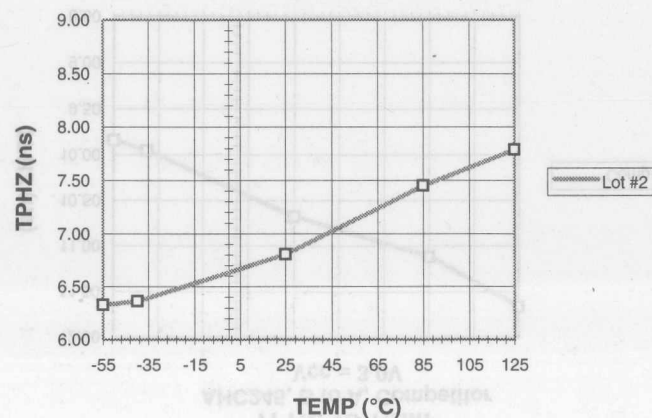




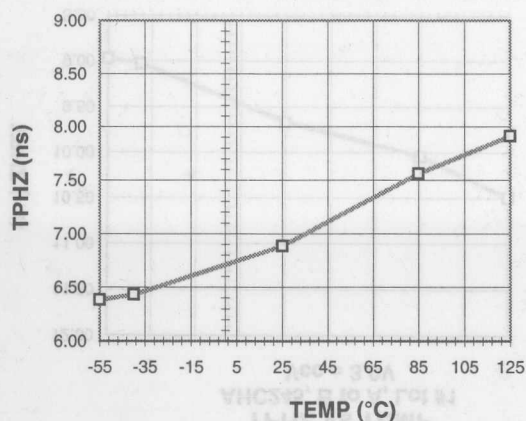
**TPHZ vs TEMP**  
AHC245, B to A, Lot #1  
Vcc = 4.5V



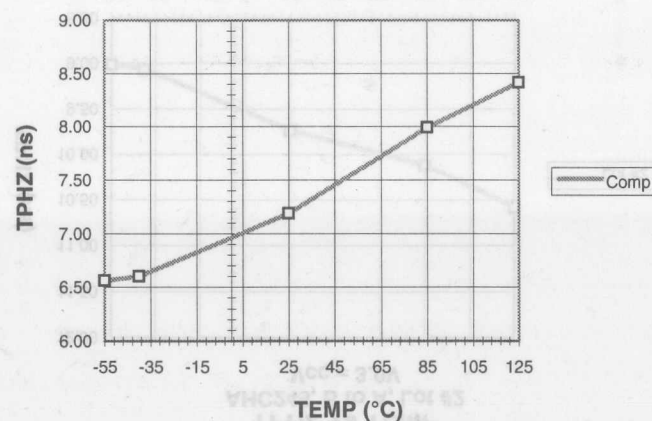
**TPHZ vs TEMP**  
AHC245, B to A, Lot #2  
Vcc = 4.5V



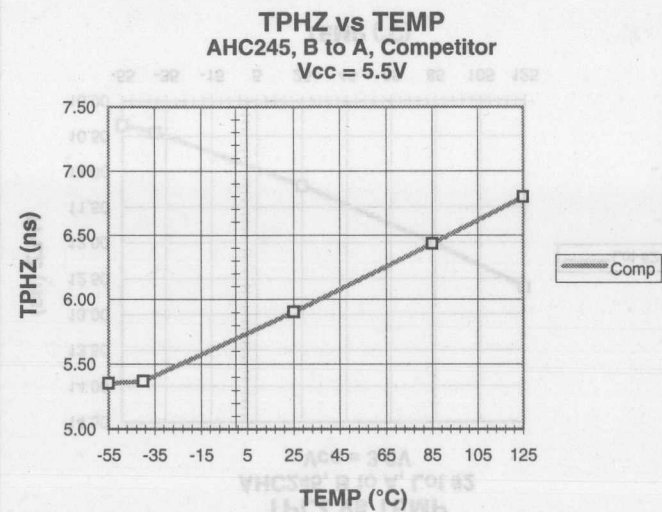
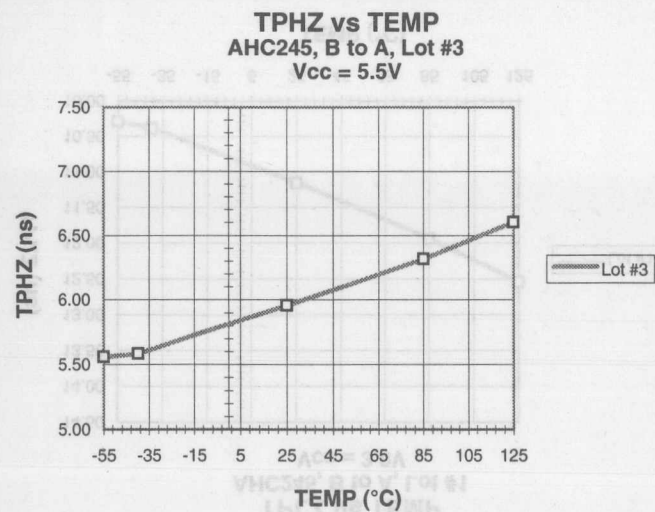
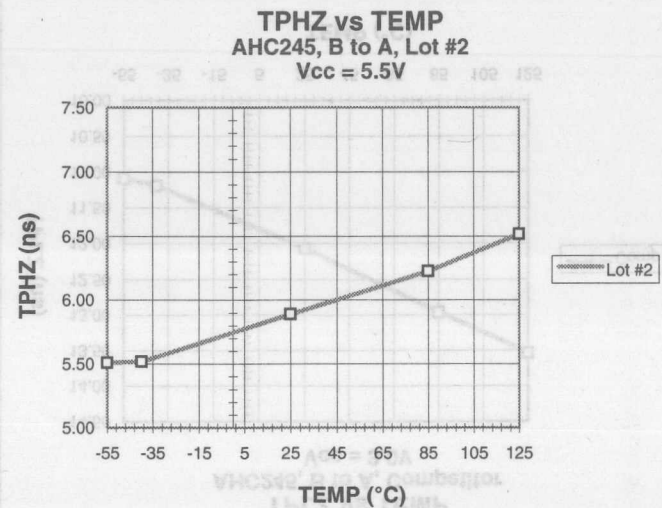
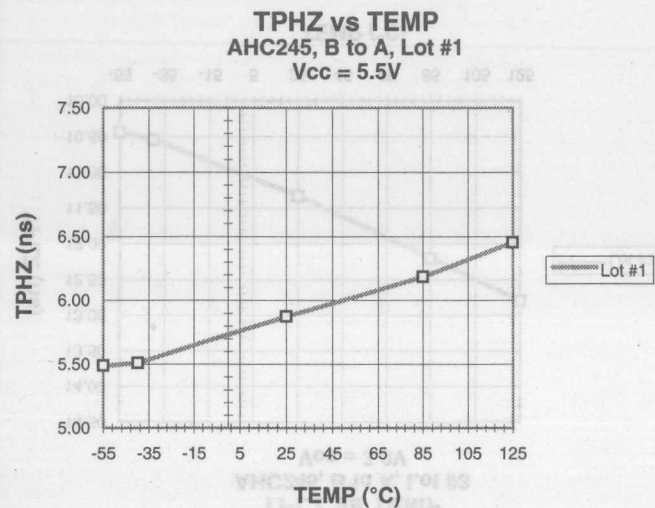
**TPHZ vs TEMP**  
AHC245, B to A, Lot #3  
Vcc = 4.5V



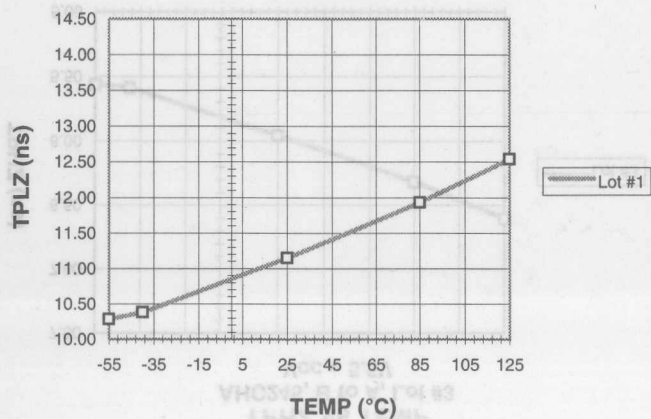
**TPHZ vs TEMP**  
AHC245, B to A, Competitor  
Vcc = 4.5V



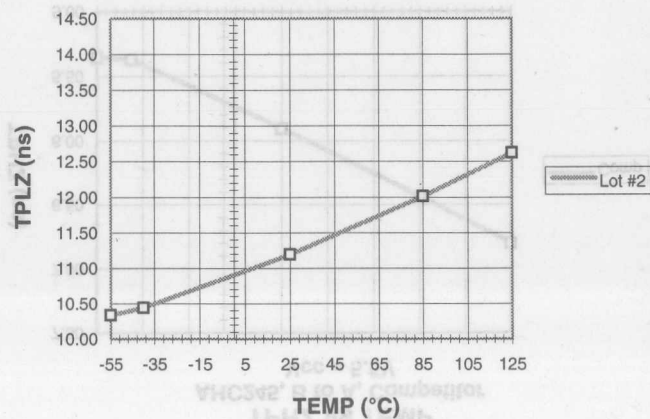




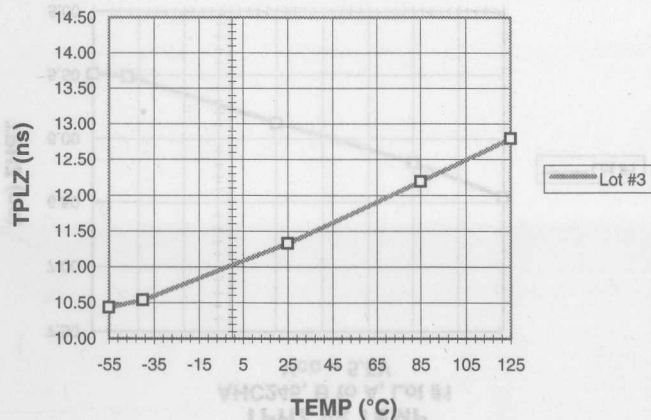
**TPLZ vs TEMP**  
AHC245, B to A, Lot #1  
Vcc = 3.0V



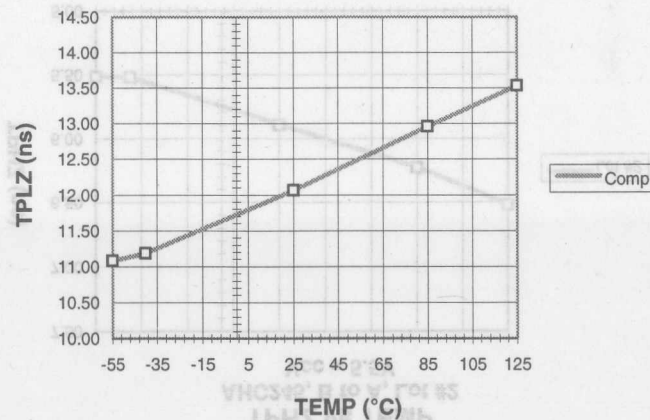
**TPLZ vs TEMP**  
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Vcc = 3.0V

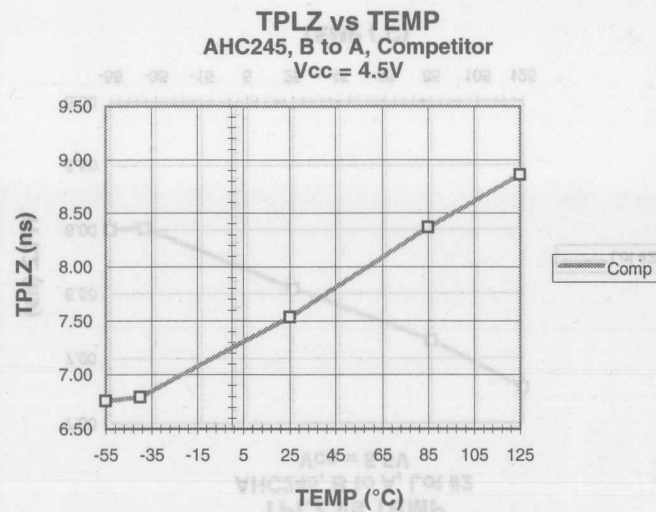
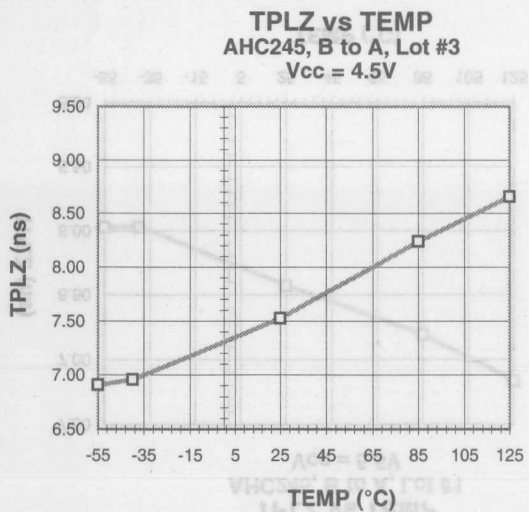
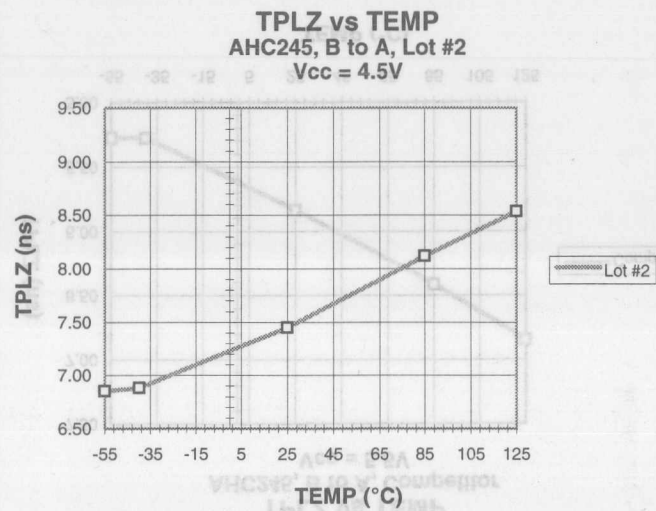
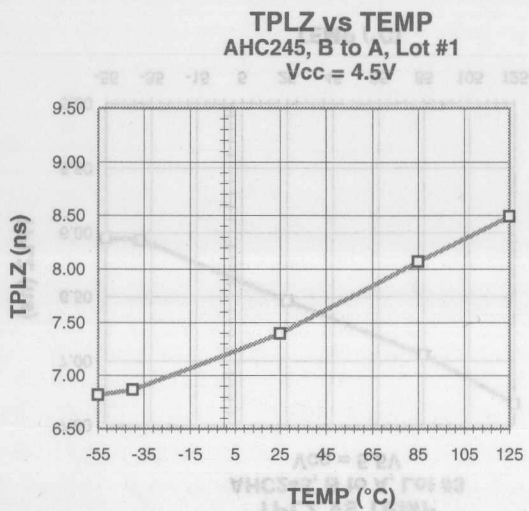


**TPLZ vs TEMP**  
AHC245, B to A, Lot #3  
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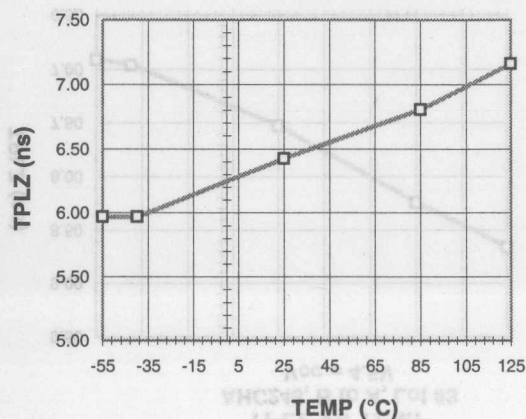


**TPLZ vs TEMP**  
AHC245, B to A, Competitor  
Vcc = 3.0V

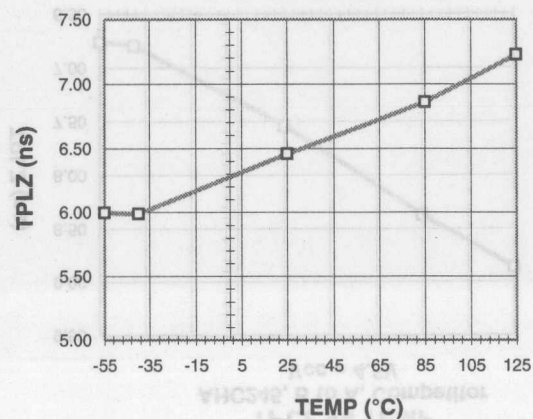




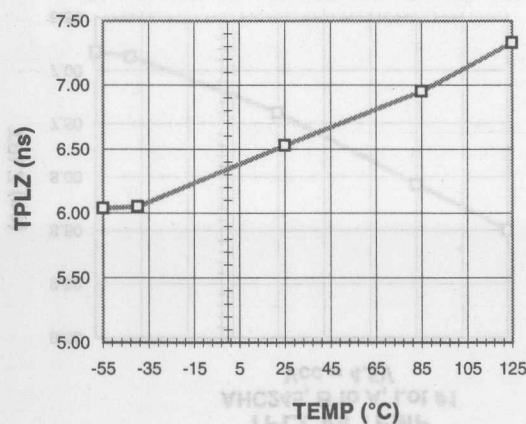
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Vcc = 5.5V



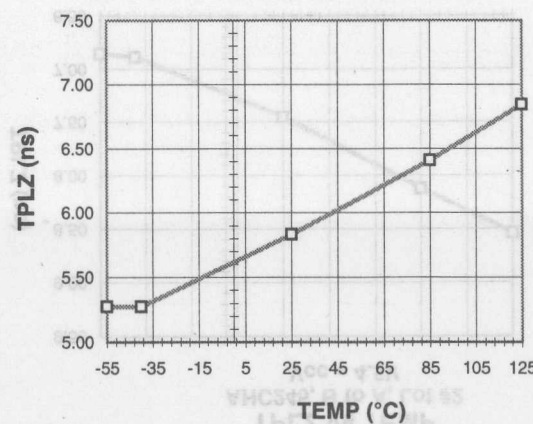
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AHC245, B to A, Lot #2  
Vcc = 5.5V



**TPLZ vs TEMP**  
AHC245, B to A, Lot #3  
Vcc = 5.5V



**TPLZ vs TEMP**  
AHC245, B to A, Competitor  
Vcc = 5.5V



<b>General Information</b>	<b>1</b>
<b>AHC Data Sheets</b>	<b>2</b>
<b>AHCT Data Sheets</b>	<b>3</b>
<b>Mechanical Data</b>	<b>4</b>
<b>AHC04 Qualification Data</b>	<b>A</b>
<b>AHCT04 Qualification Data</b>	<b>B</b>
<b>AHC245 Qualification Data</b>	<b>C</b>
<b>AHCT245 Qualification Data</b>	<b>D</b>



**D AHCT245 Qualification Data**

AHCT245 Qualification Data

C

AHCT245 Qualification Data

B

AHCT245 Qualification Data

A

AHCT245 Qualification Data

4

Mechanical Data

3

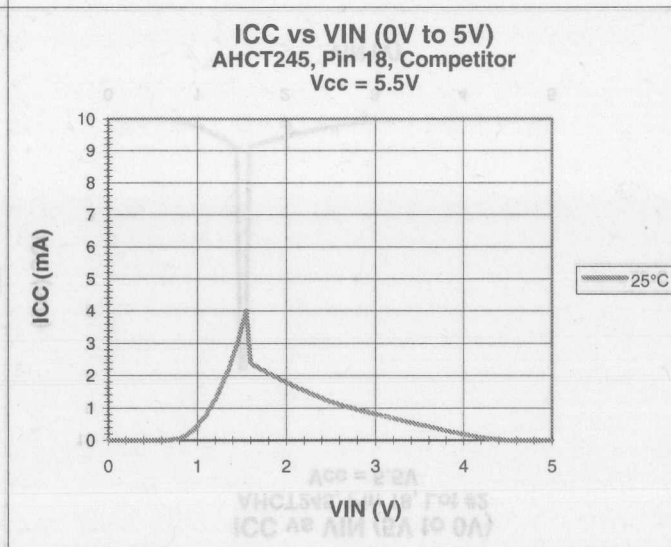
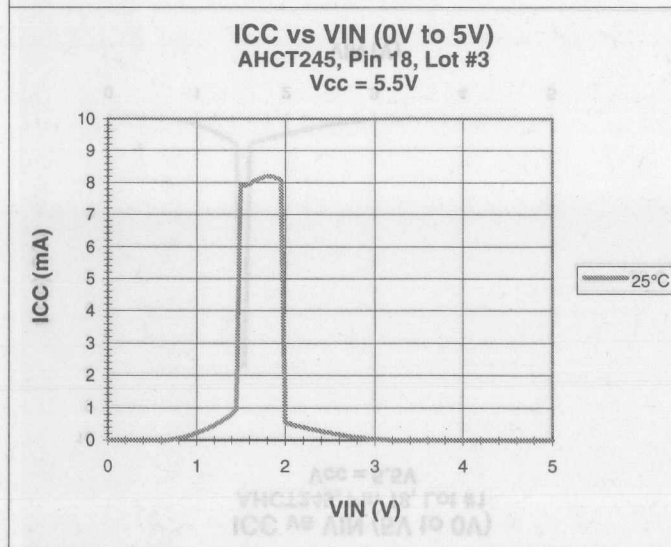
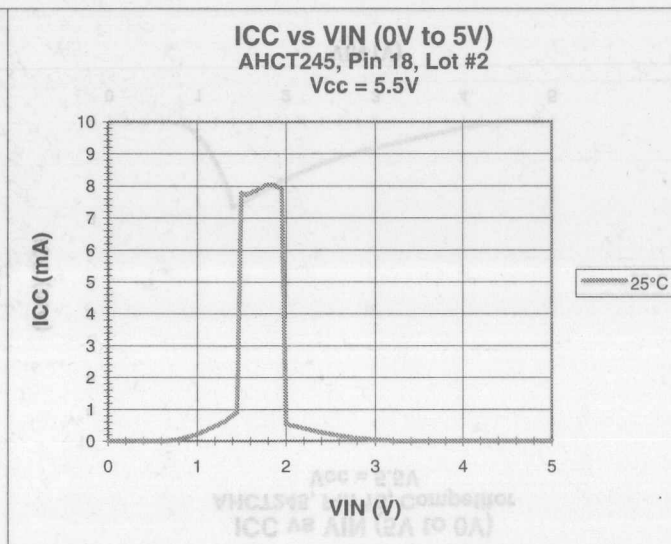
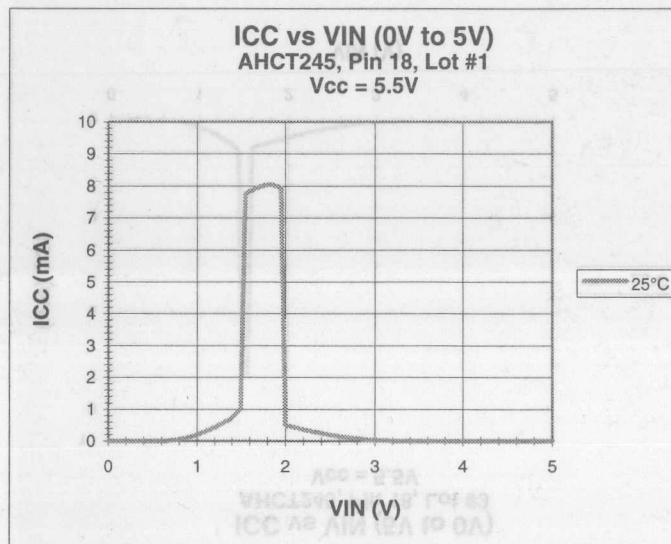
AHCT Data Sheets

2

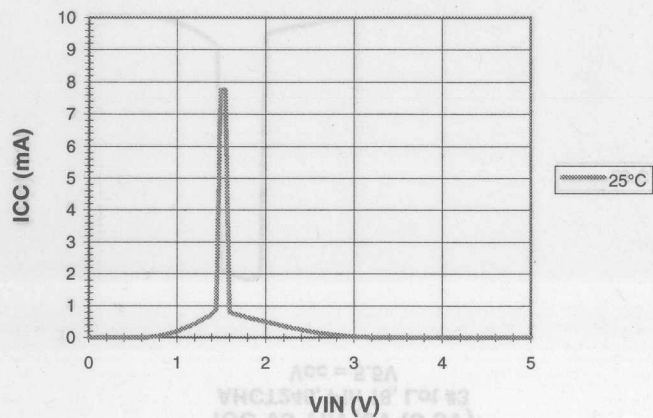
AHCT Data Sheets

1

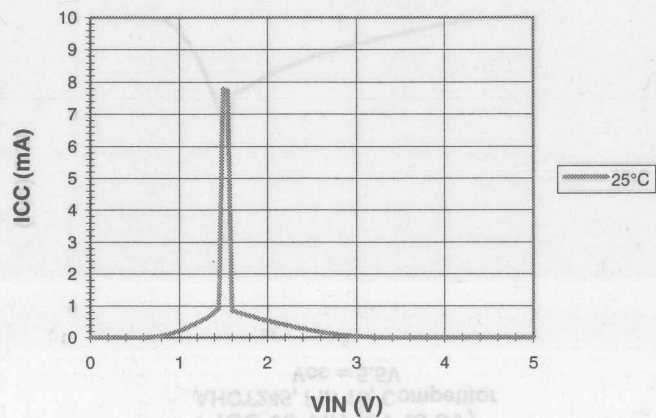
General Information



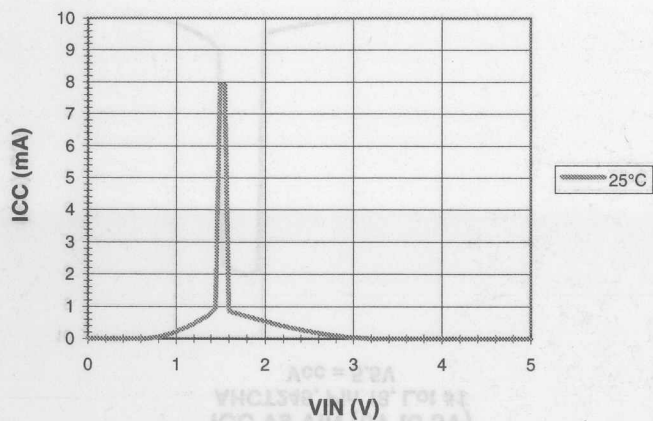
**ICC vs VIN (5V to 0V)**  
**AHCT245, Pin 18, Lot #1**  
**Vcc = 5.5V**



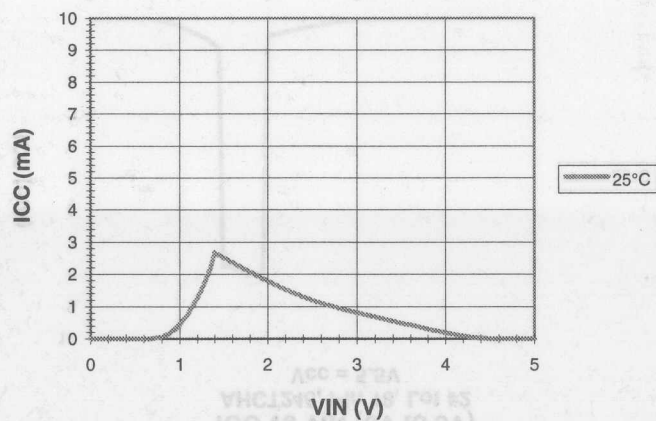
**ICC vs VIN (5V to 0V)**  
**AHCT245, Pin 18, Lot #2**  
**Vcc = 5.5V**



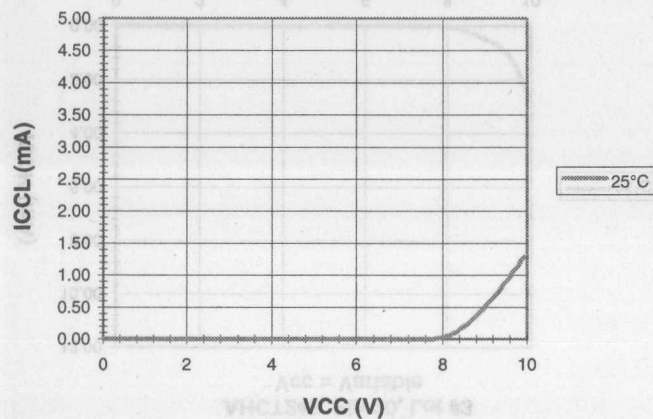
**ICC vs VIN (5V to 0V)**  
**AHCT245, Pin 18, Lot #3**  
**Vcc = 5.5V**



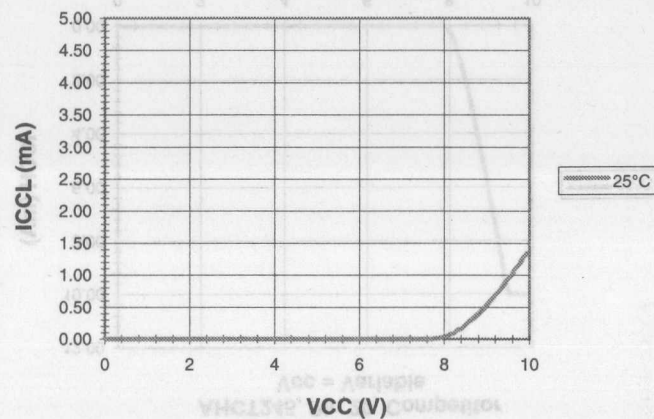
**ICC vs VIN (5V to 0V)**  
**AHCT245, Pin 18, Competitor**  
**Vcc = 5.5V**



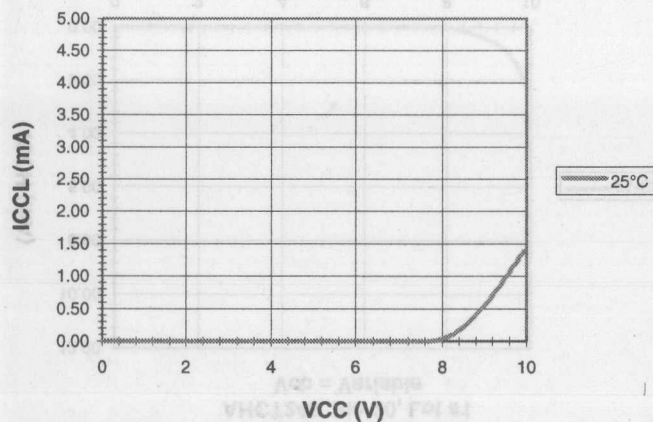
**ICCL vs VCC**  
**AHCT245, Pin 20, Lot #1**  
**Vcc = Variable**



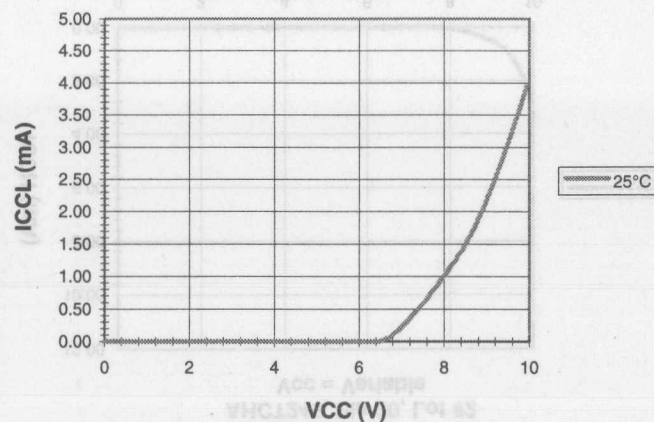
**ICCL vs VCC**  
**AHCT245, Pin 20, Lot #2**  
**Vcc = Variable**



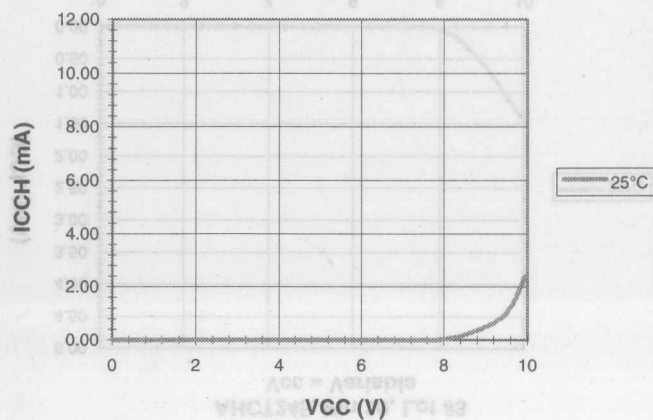
**ICCL vs VCC**  
**AHCT245, Pin 20, Lot #3**  
**Vcc = Variable**



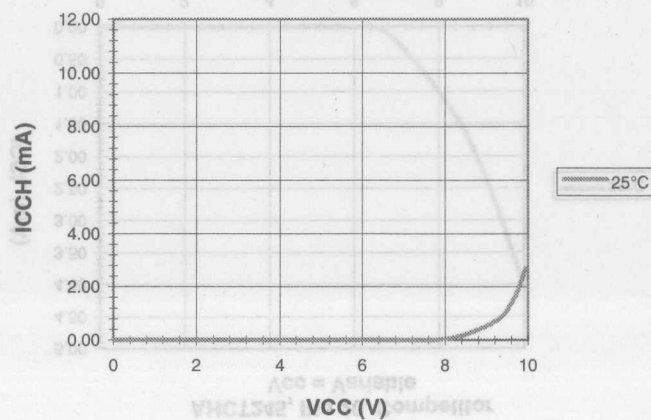
**ICCL vs VCC**  
**AHCT245, Pin 20, Competitor**  
**Vcc = Variable**



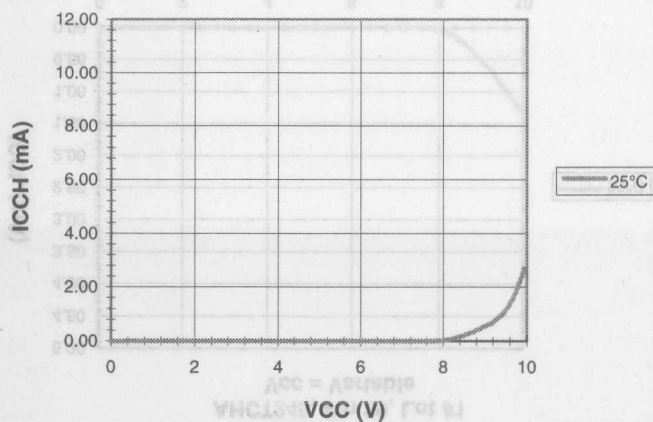
**ICCH vs VCC**  
AHCT245, Pin 20, Lot #1  
Vcc = Variable



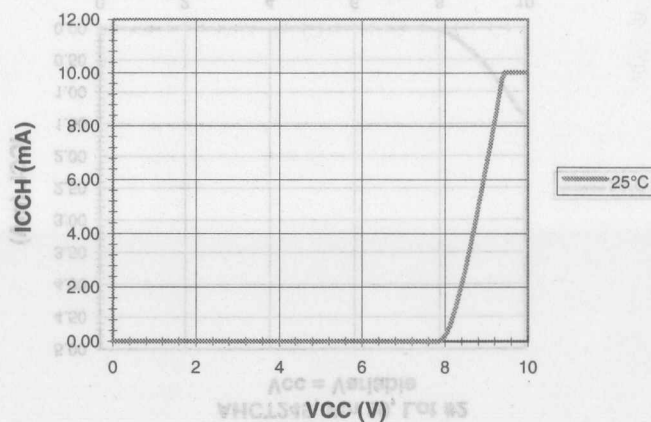
**ICCH vs VCC**  
AHCT245, Pin 20, Lot #2  
Vcc = Variable



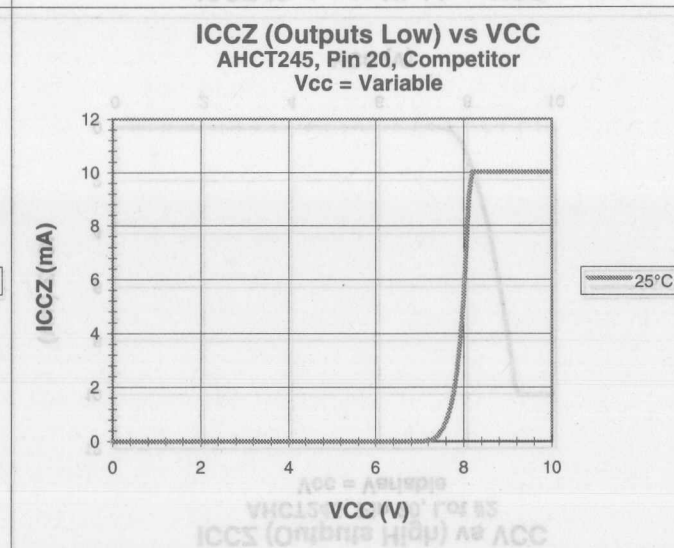
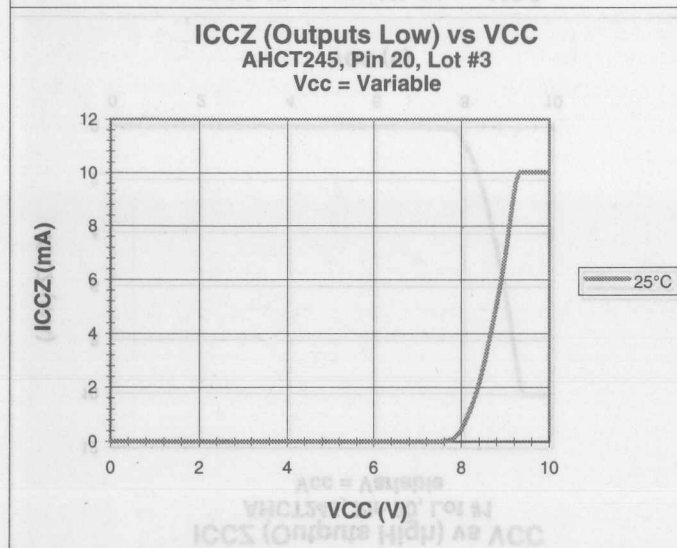
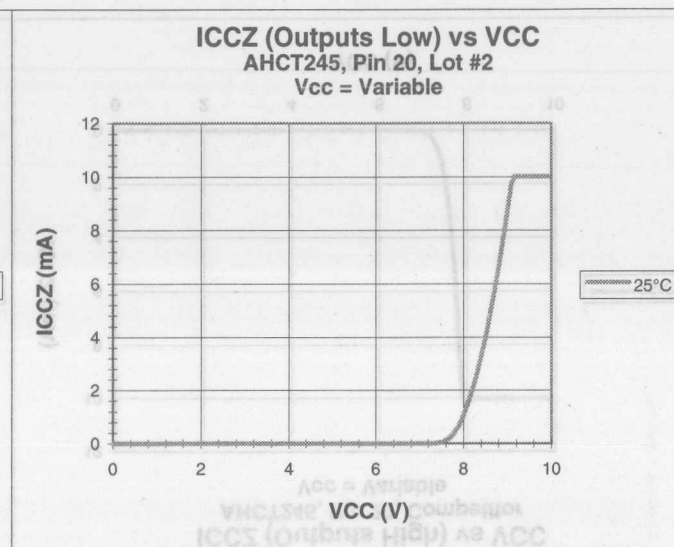
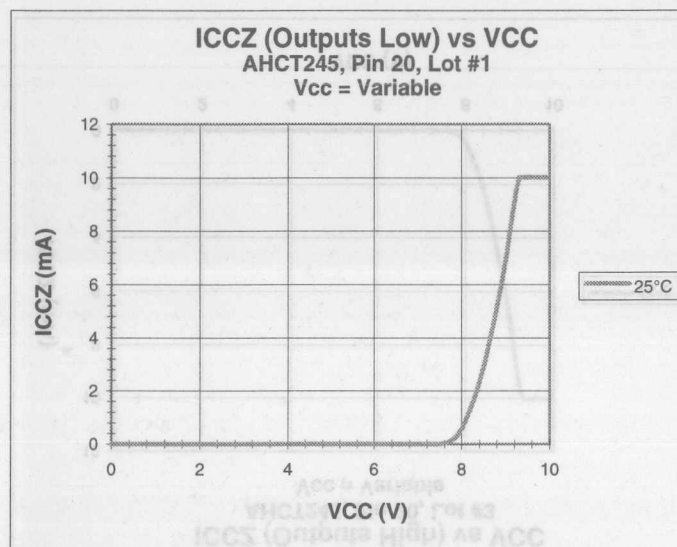
**ICCH vs VCC**  
AHCT245, Pin 20, Lot #3  
Vcc = Variable



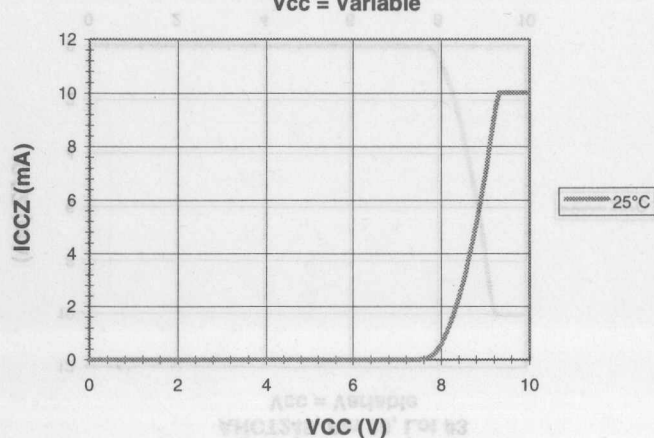
**ICCH vs VCC**  
AHCT245, Pin 20, Competitor  
Vcc = Variable



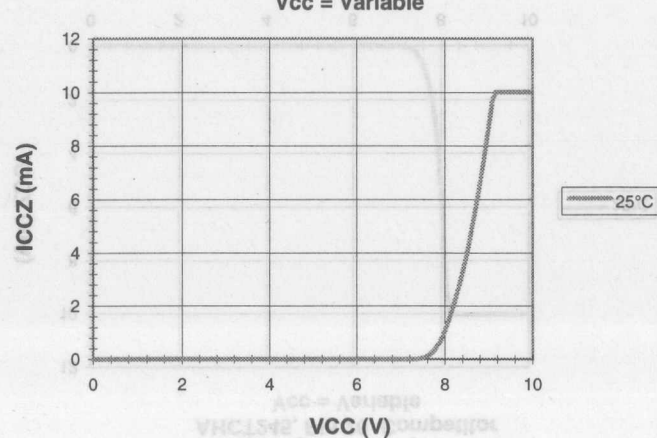




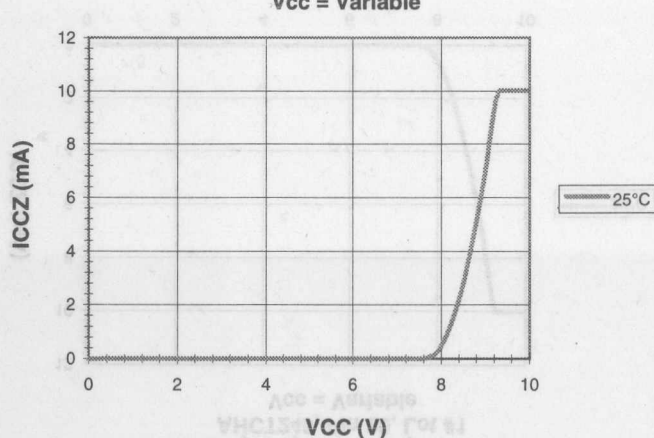
**ICCZ (Outputs High) vs VCC**  
AHCT245, Pin 20, Lot #1  
Vcc = Variable



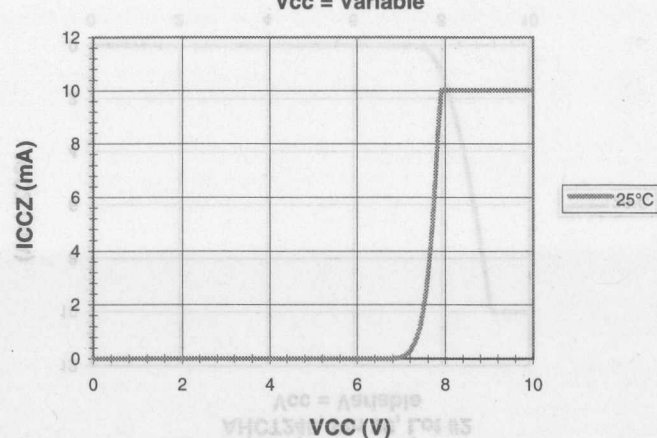
**ICCZ (Outputs High) vs VCC**  
AHCT245, Pin 20, Lot #2  
Vcc = Variable

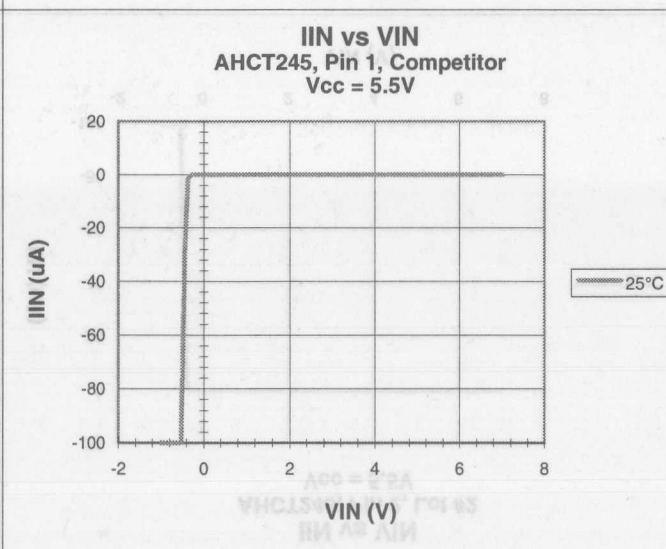
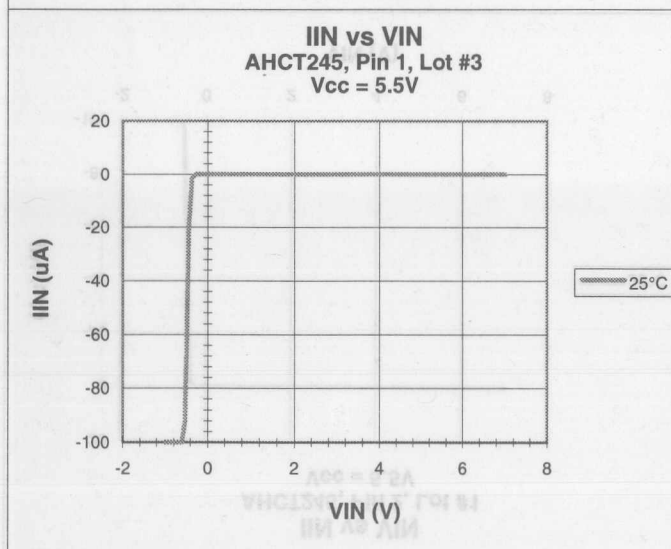
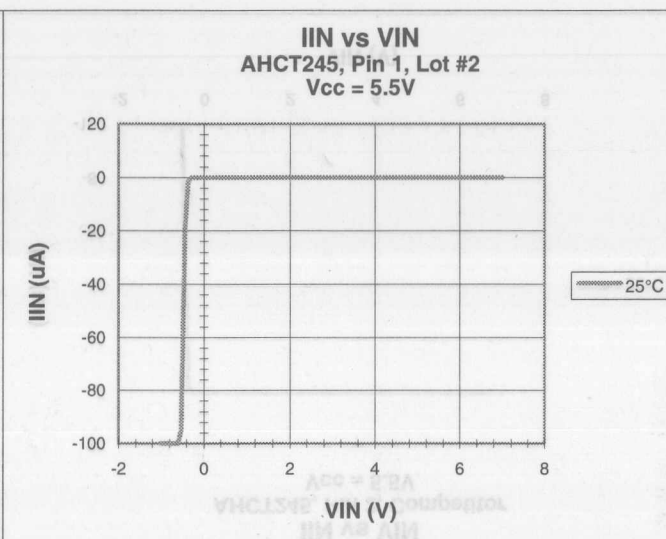
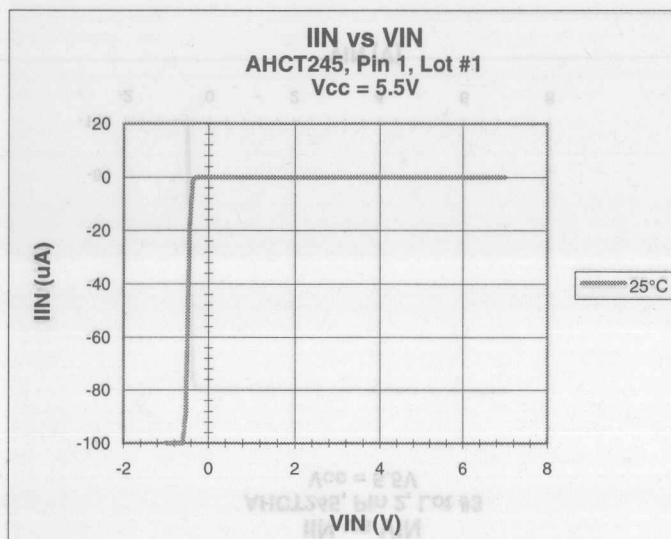


**ICCZ (Outputs High) vs VCC**  
AHCT245, Pin 20, Lot #3  
Vcc = Variable

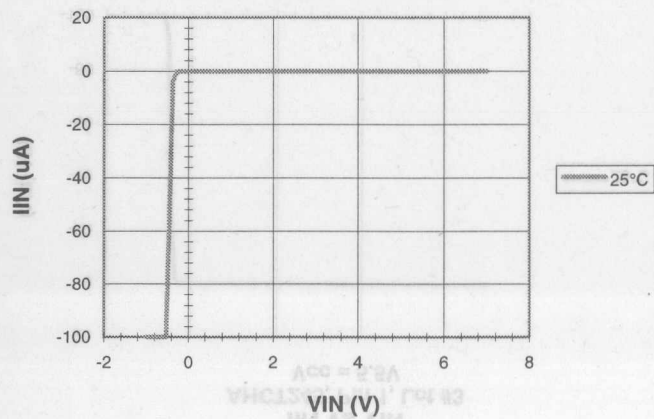


**ICCZ (Outputs High) vs VCC**  
AHCT245, Pin 20, Competitor  
Vcc = Variable

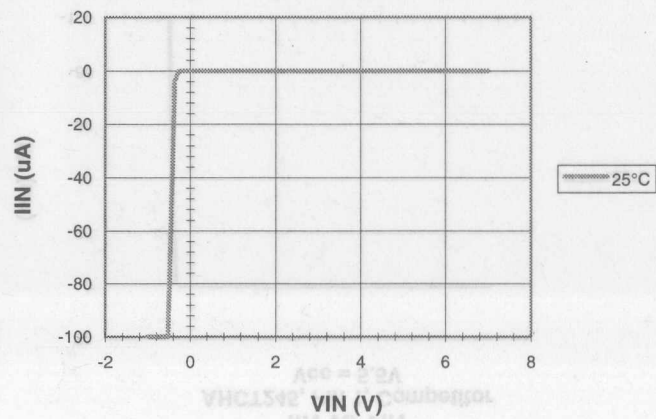




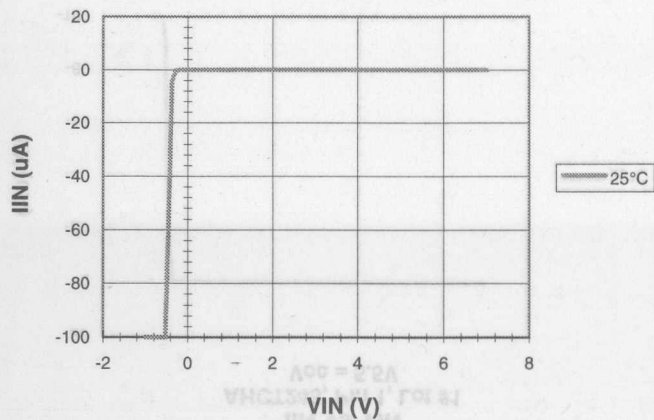
**IIN vs VIN**  
AHCT245, Pin 2, Lot #1  
Vcc = 5.5V



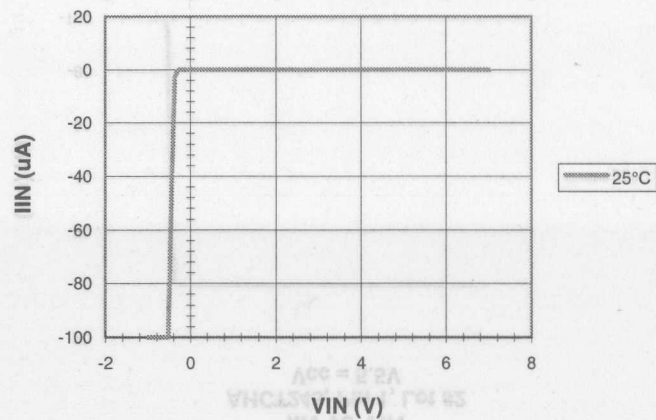
**IIN vs VIN**  
AHCT245, Pin 2, Lot #2  
Vcc = 5.5V

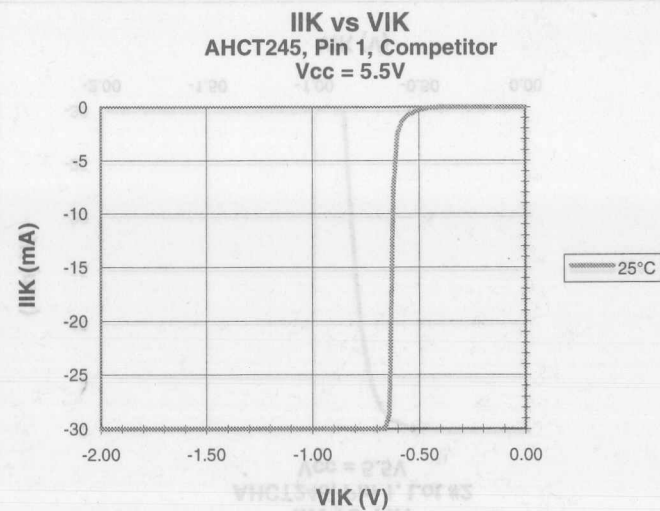
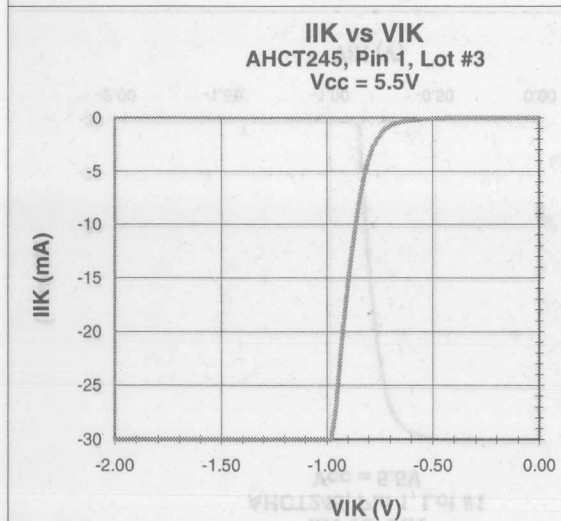
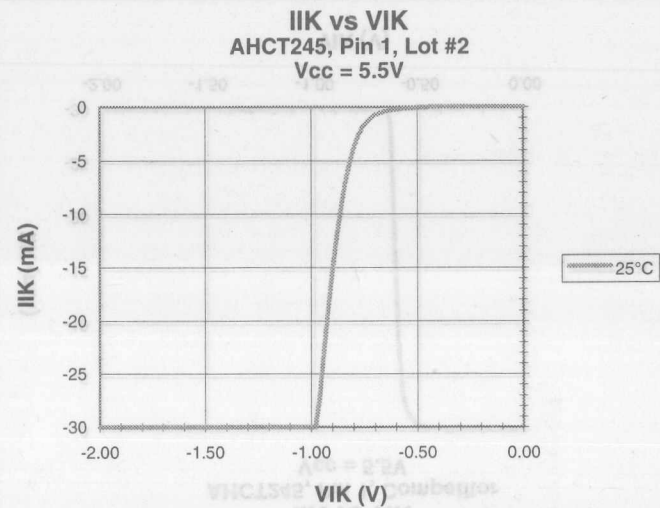
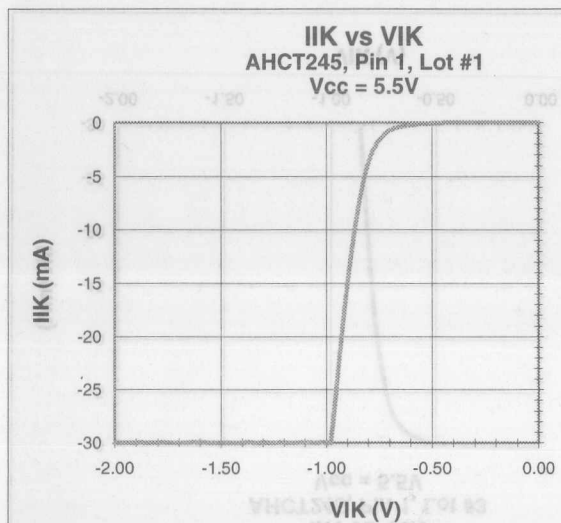


**IIN vs VIN**  
AHCT245, Pin 2, Lot #3  
Vcc = 5.5V

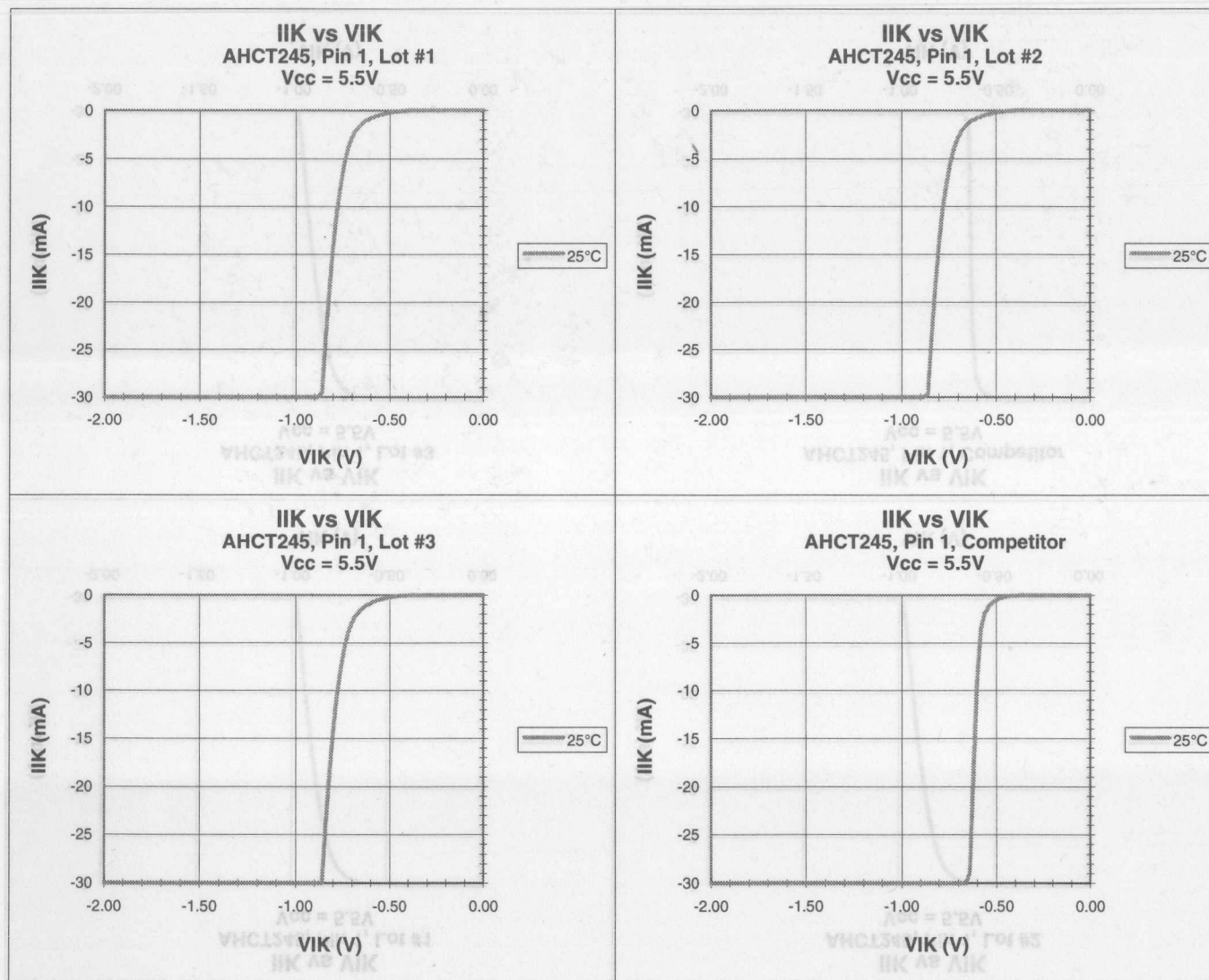


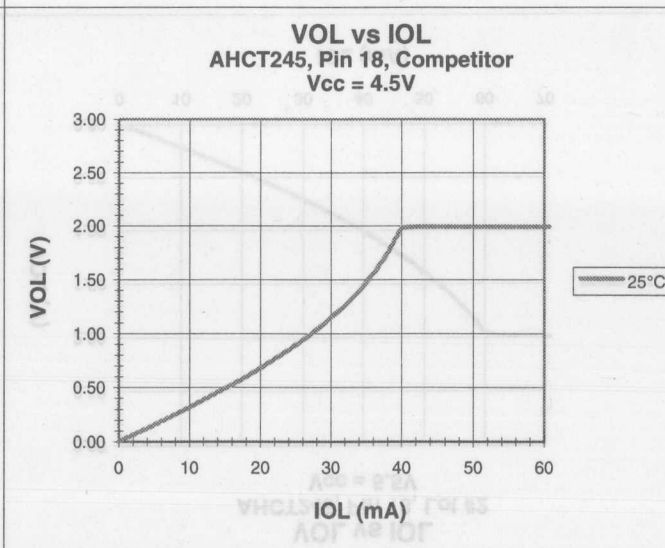
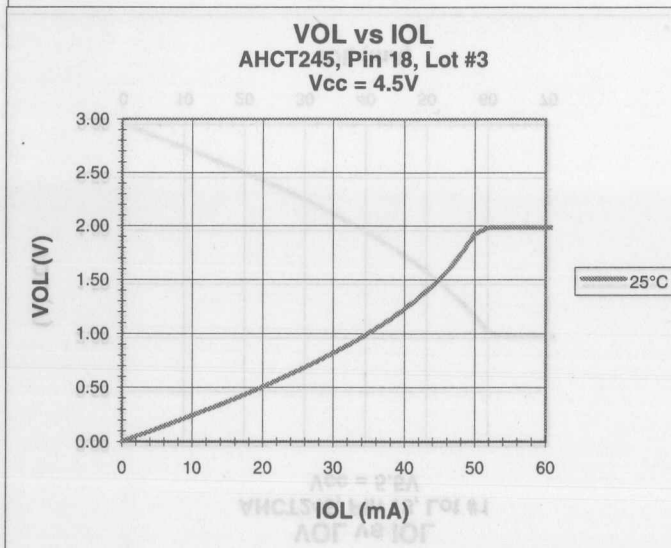
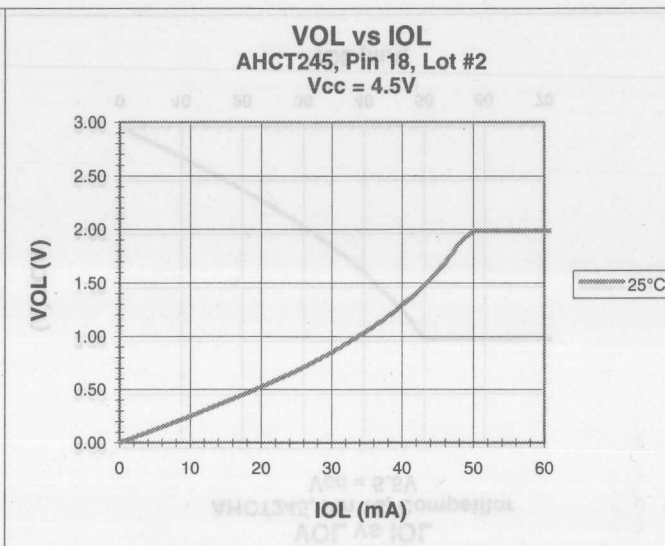
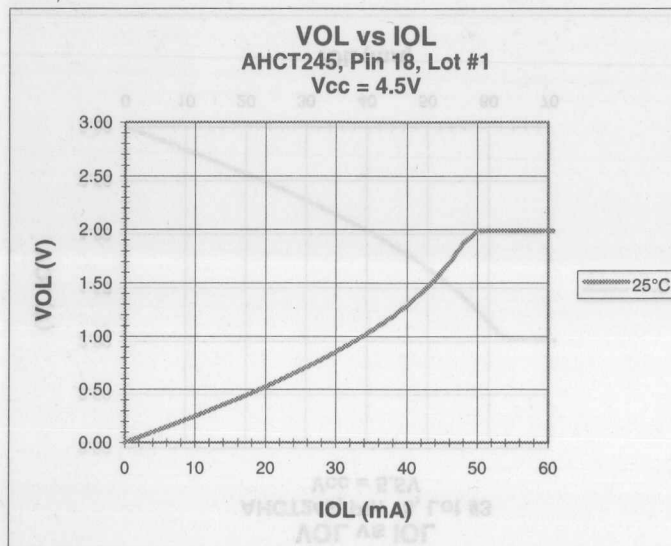
**IIN vs VIN**  
AHCT245, Pin 2, Competitor  
Vcc = 5.5V



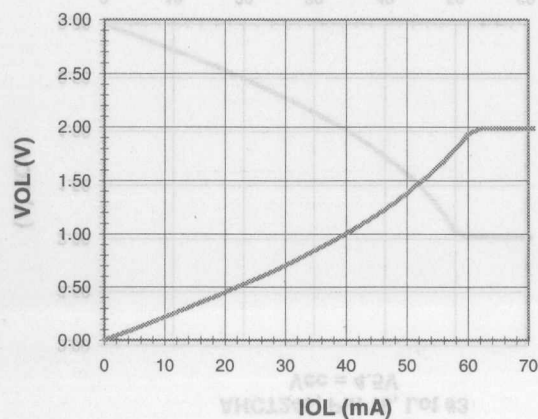




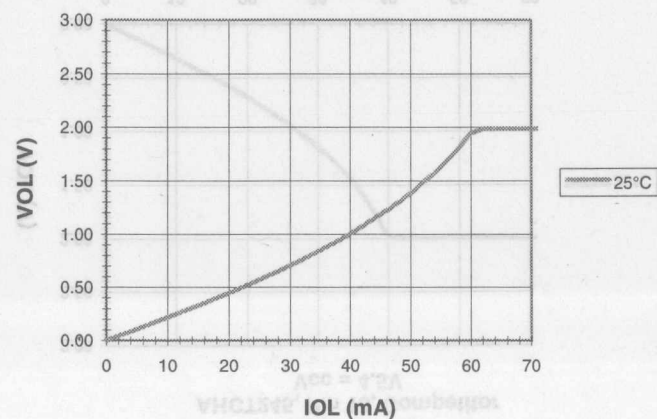




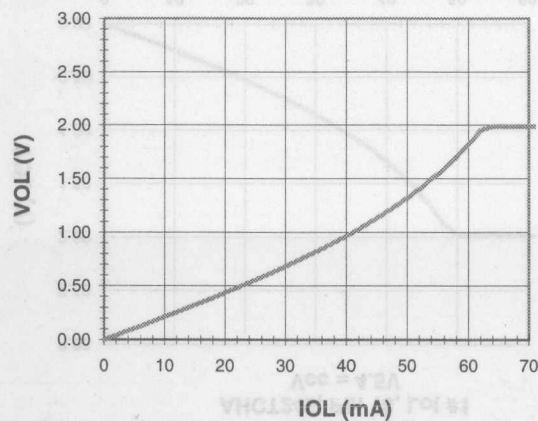
**VOL vs IOL**  
AHCT245, Pin 18, Lot #1  
Vcc = 5.5V



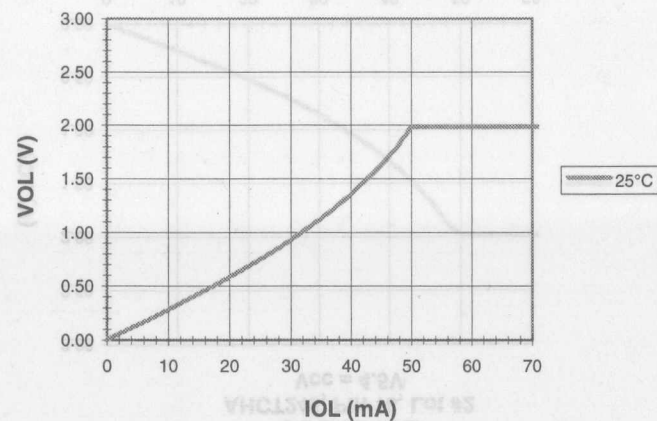
**VOL vs IOL**  
AHCT245, Pin 18, Lot #2  
Vcc = 5.5V



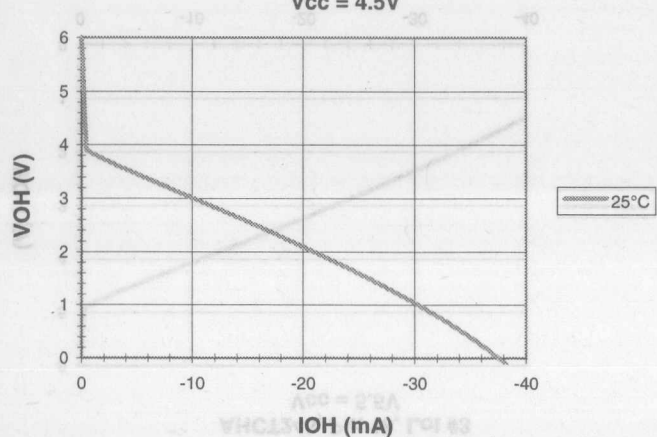
**VOL vs IOL**  
AHCT245, Pin 18, Lot #3  
Vcc = 5.5V



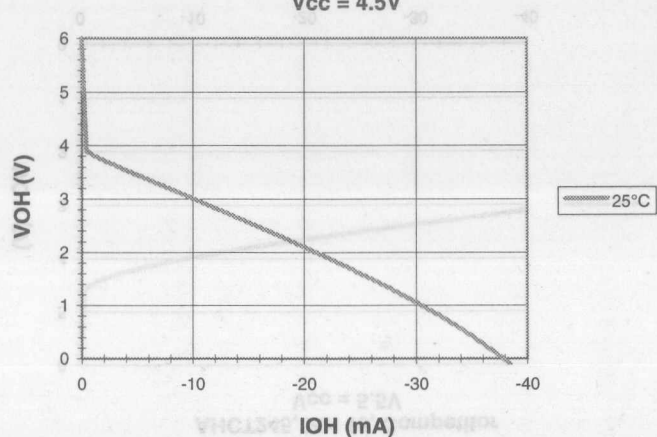
**VOL vs IOL**  
AHCT245, Pin 18, Competitor  
Vcc = 5.5V



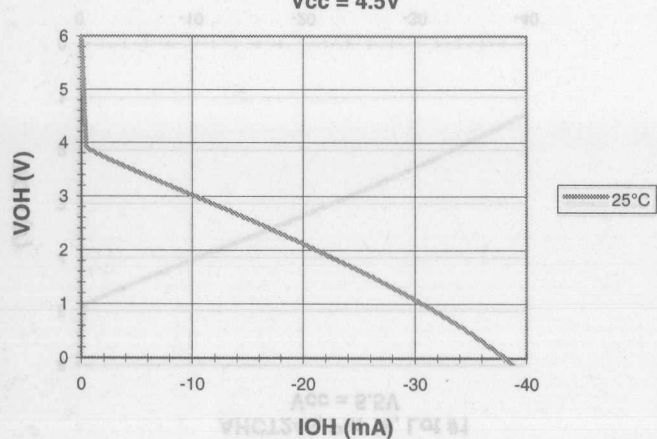
**VOH vs IOH**  
**AHCT245, Pin 18, Lot #1**  
**Vcc = 4.5V**



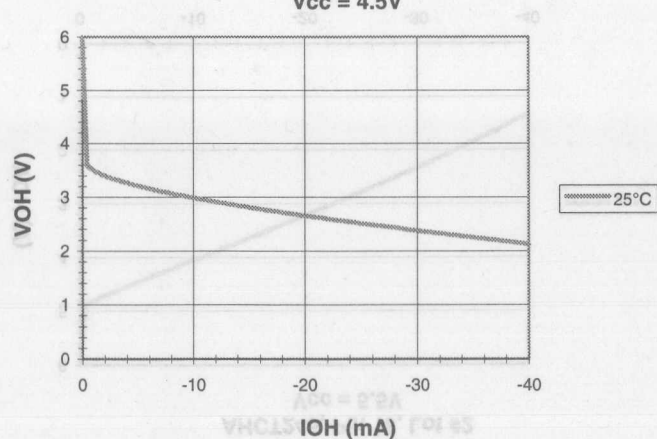
**VOH vs IOH**  
**AHCT245, Pin 18, Lot #2**  
**Vcc = 4.5V**



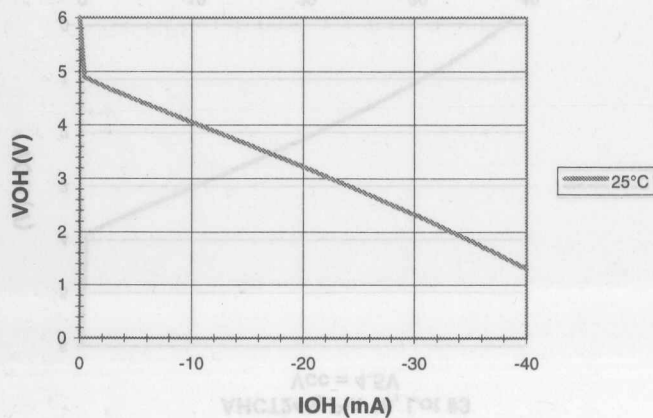
**VOH vs IOH**  
**AHCT245, Pin 18, Lot #3**  
**Vcc = 4.5V**



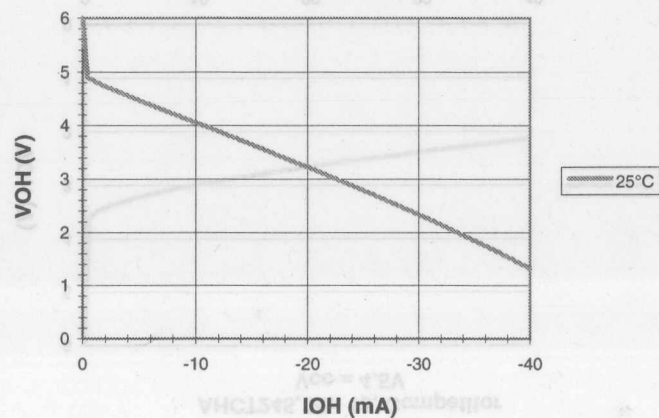
**VOH vs IOH**  
**AHCT245, Pin 18, Competitor**  
**Vcc = 4.5V**



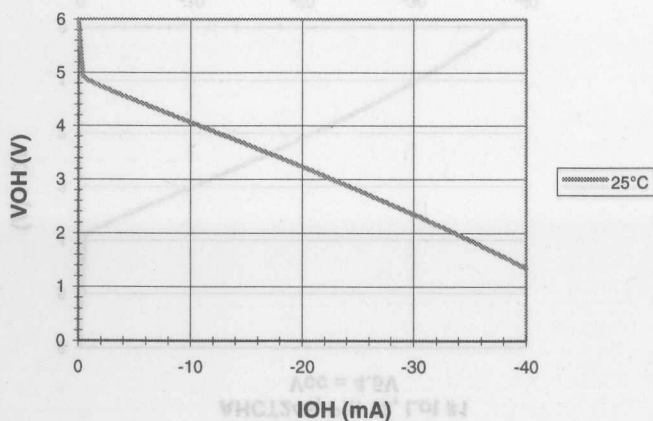
**VOH vs IOH**  
AHCT245, Pin 18, Lot #1  
Vcc = 5.5V



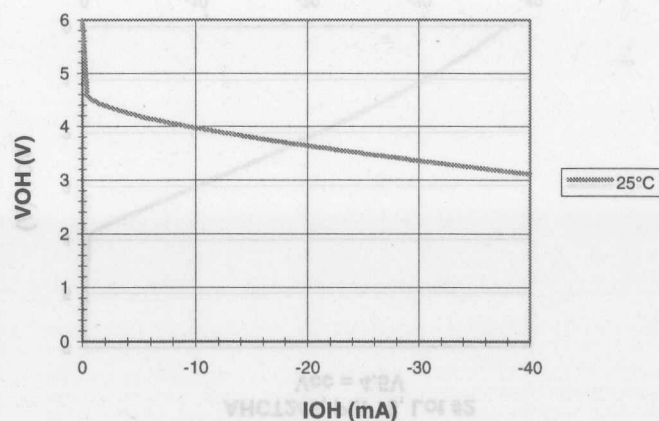
**VOH vs IOH**  
AHCT245, Pin 18, Lot #2  
Vcc = 5.5V



**VOH vs IOH**  
AHCT245, Pin 18, Lot #3  
Vcc = 5.5V

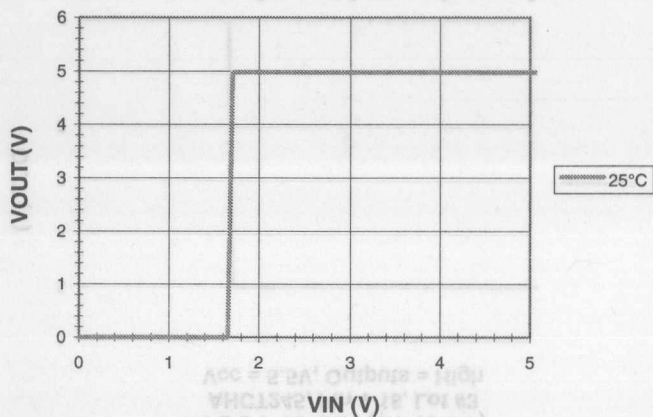


**VOH vs IOH**  
AHCT245, Pin 18, Competitor  
Vcc = 5.5V

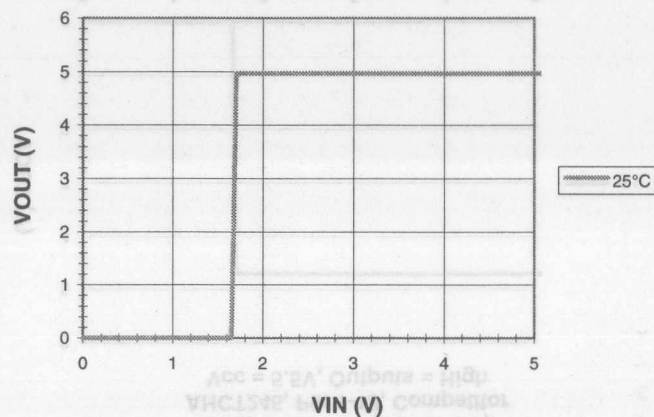




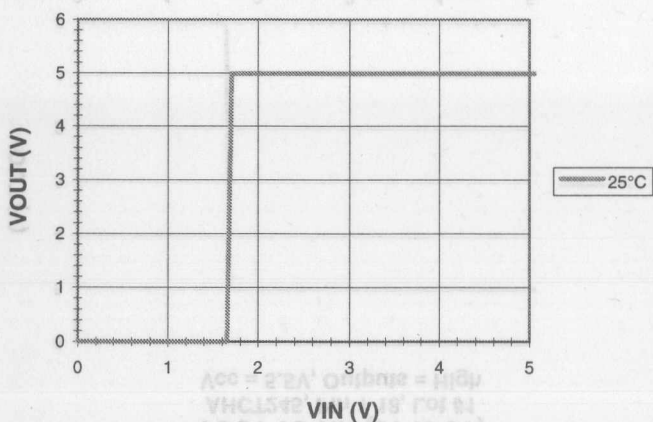
**VOUT vs VIN (0V to 5V)**  
**AHCT245, Pin 1-18, Lot #1**  
**Vcc = 5.5V, Outputs = Low**



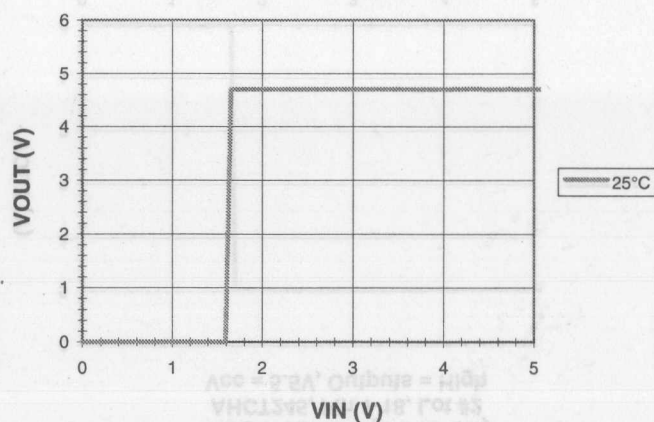
**VOUT vs VIN (0V to 5V)**  
**AHCT245, Pin 1-18, Lot #2**  
**Vcc = 5.5V, Outputs = Low**



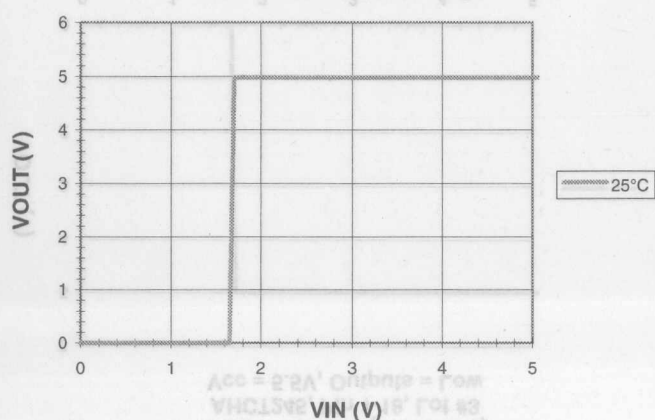
**VOUT vs VIN (0V to 5V)**  
**AHCT245, Pin 1-18, Lot #3**  
**Vcc = 5.5V, Outputs = Low**



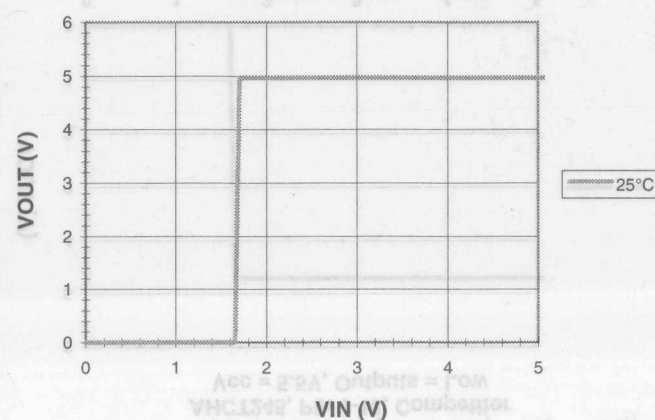
**VOUT vs VIN (0V to 5V)**  
**AHCT245, Pin 1-18, Competitor**  
**Vcc = 5.5V, Outputs = Low**



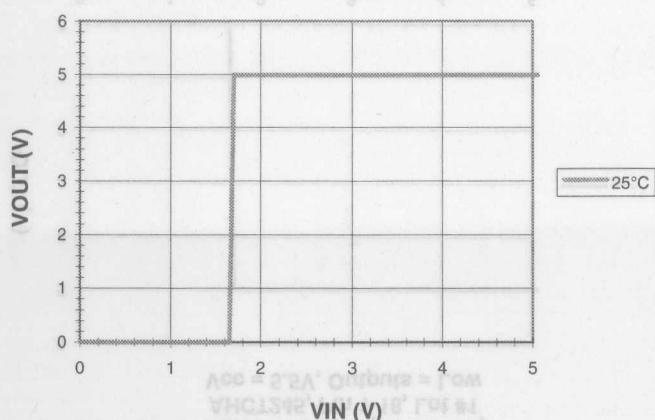
**VOUT vs VIN (0V to 5V)**  
AHCT245, Pin 1-18, Lot #1  
Vcc = 5.5V, Outputs = High



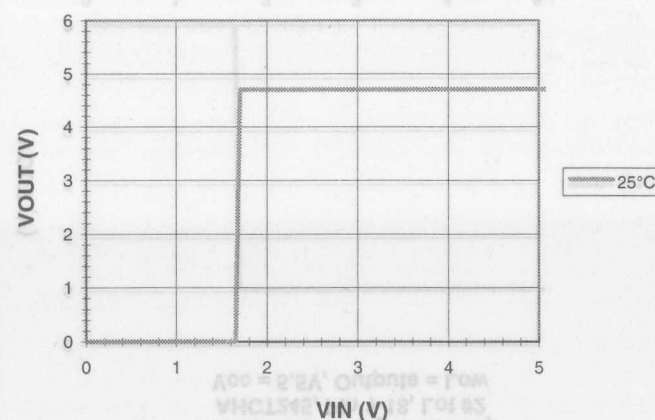
**VOUT vs VIN (0V to 5V)**  
AHCT245, Pin 1-18, Lot #2  
Vcc = 5.5V, Outputs = High



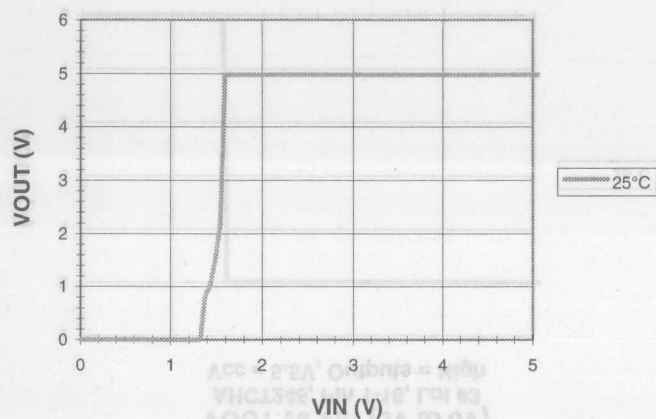
**VOUT vs VIN (0V to 5V)**  
AHCT245, Pin 1-18, Lot #3  
Vcc = 5.5V, Outputs = High



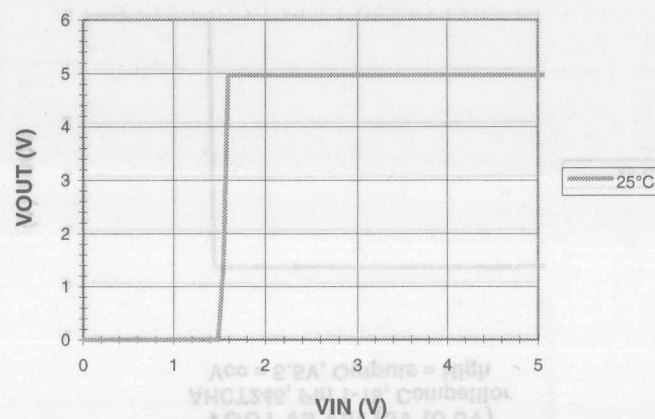
**VOUT vs VIN (0V to 5V)**  
AHCT245, Pin 1-18, Competitor  
Vcc = 5.5V, Outputs = High



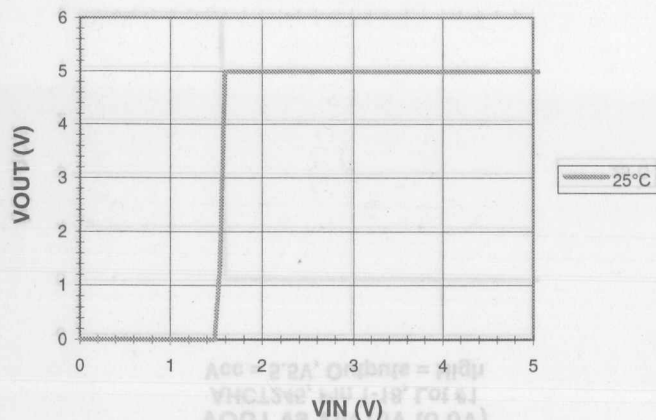
**VOUT vs VIN (5V to 0V)**  
**AHCT245, Pin 1-18, Lot #1**  
**Vcc = 5.5V, Outputs = Low**



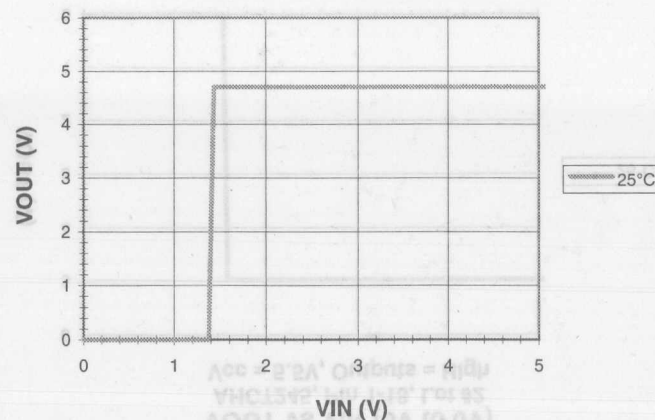
**VOUT vs VIN (5V to 0V)**  
**AHCT245, Pin 1-18, Lot #2**  
**Vcc = 5.5V, Outputs = Low**



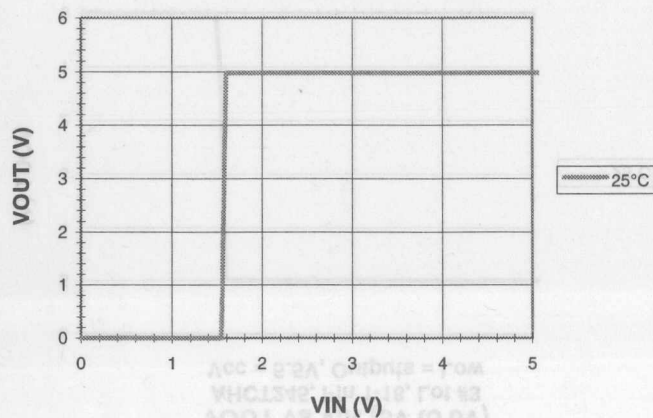
**VOUT vs VIN (5V to 0V)**  
**AHCT245, Pin 1-18, Lot #3**  
**Vcc = 5.5V, Outputs = Low**



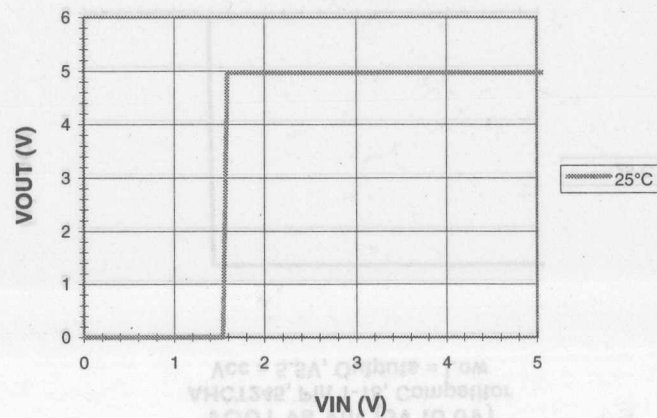
**VOUT vs VIN (5V to 0V)**  
**AHCT245, Pin 1-18, Competitor**  
**Vcc = 5.5V, Outputs = Low**



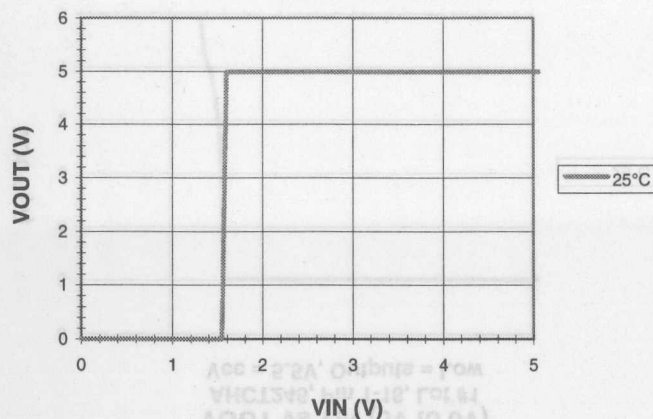
**VOUT vs VIN (5V to 0V)**  
AHCT245, Pin 1-18, Lot #1  
Vcc = 5.5V, Outputs = High



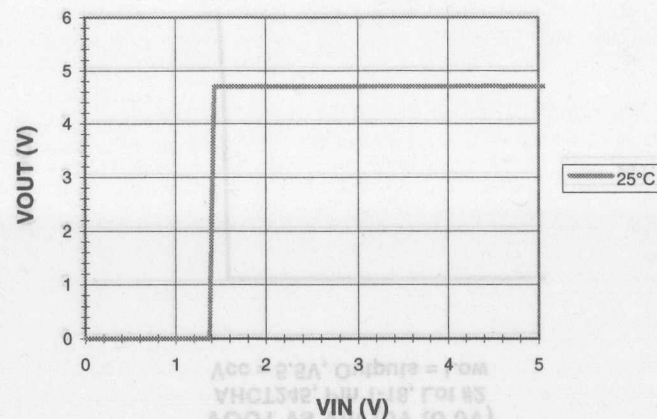
**VOUT vs VIN (5V to 0V)**  
AHCT245, Pin 1-18, Lot #2  
Vcc = 5.5V, Outputs = High

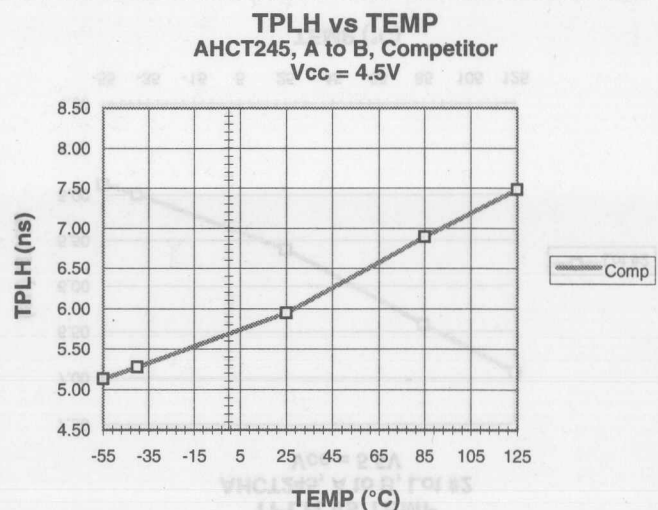
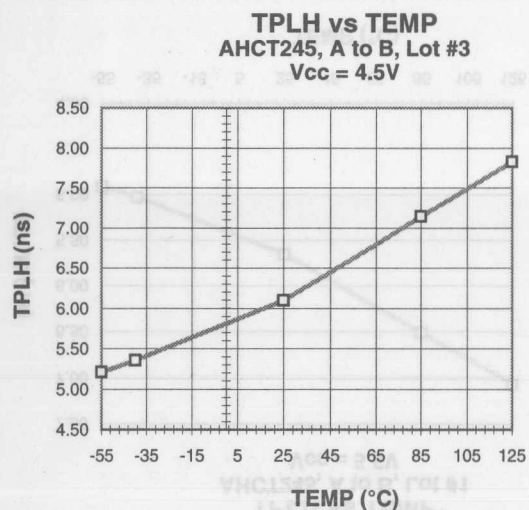
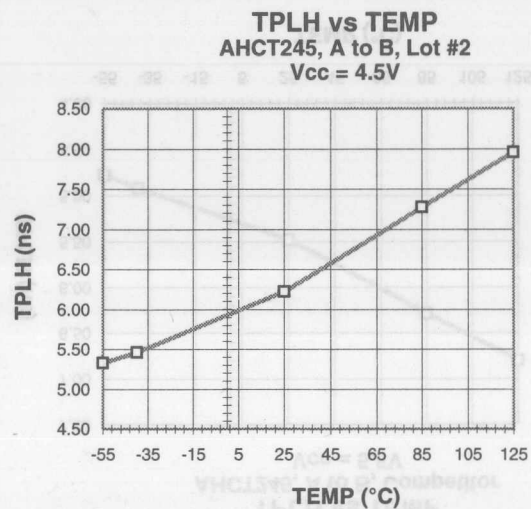
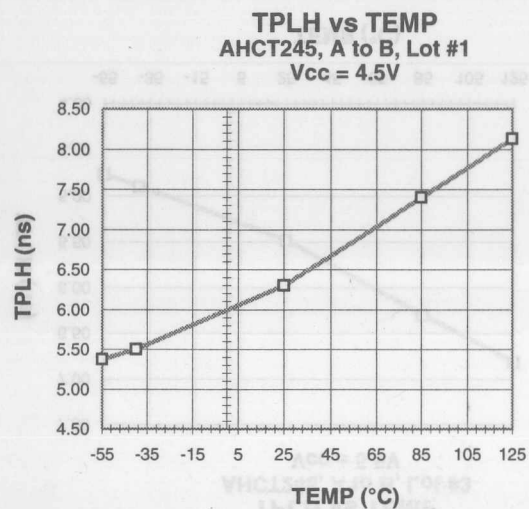


**VOUT vs VIN (5V to 0V)**  
AHCT245, Pin 1-18, Lot #3  
Vcc = 5.5V, Outputs = High



**VOUT vs VIN (5V to 0V)**  
AHCT245, Pin 1-18, Competitor  
Vcc = 5.5V, Outputs = High

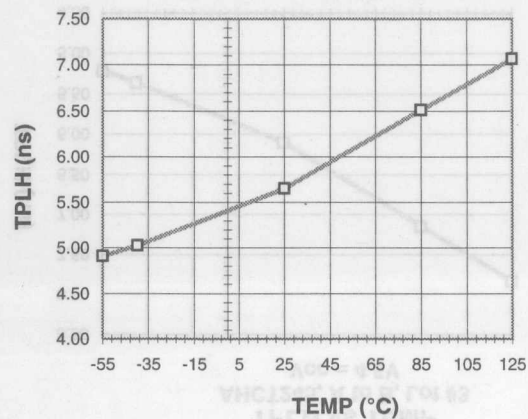






**TPLH vs TEMP**  
AHCT245, A to B, Lot #1

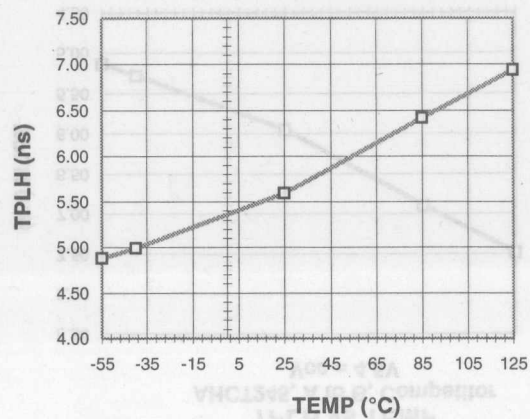
Vcc = 5.5V



Lot #1

**TPLH vs TEMP**  
AHCT245, A to B, Lot #2

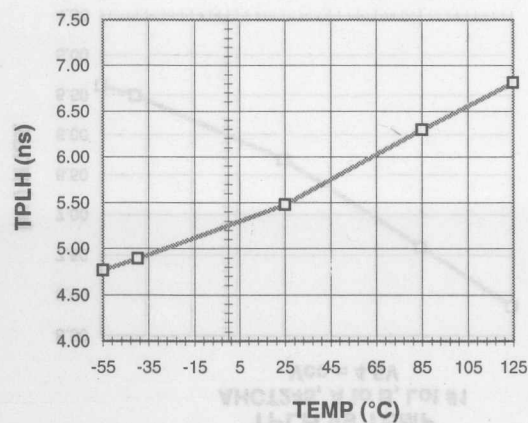
Vcc = 5.5V



Lot #2

**TPLH vs TEMP**  
AHCT245, A to B, Lot #3

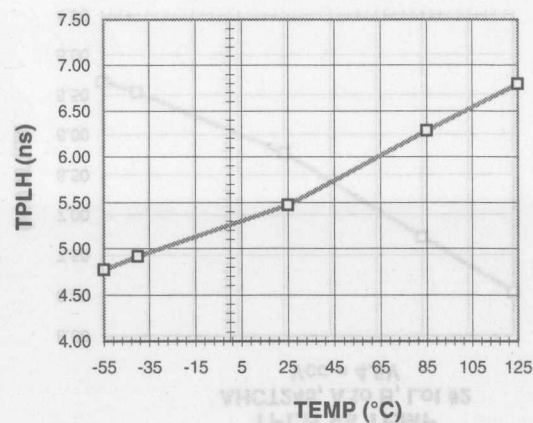
Vcc = 5.5V



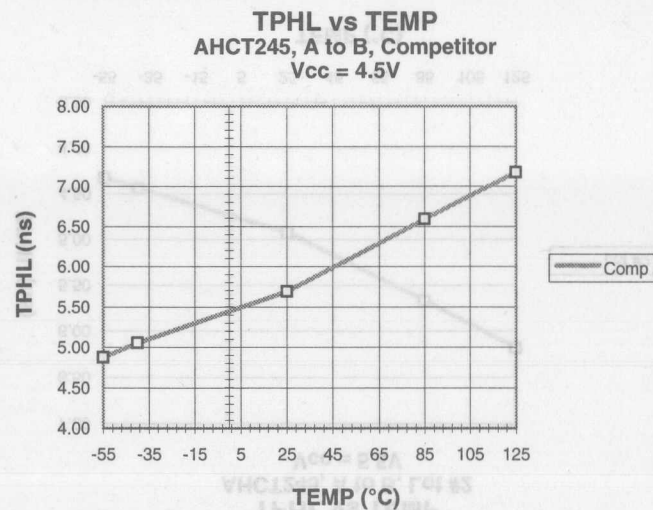
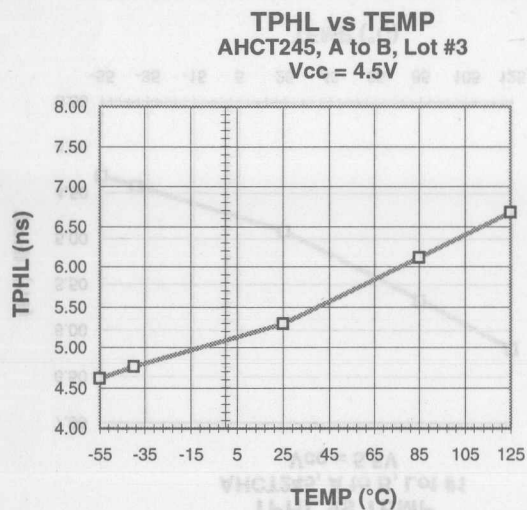
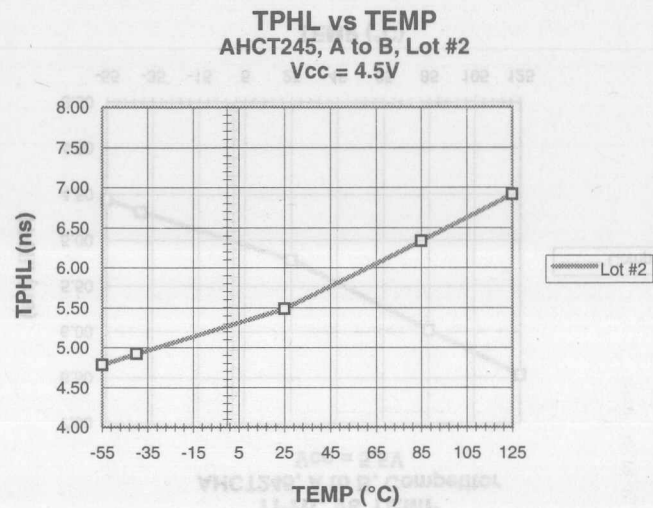
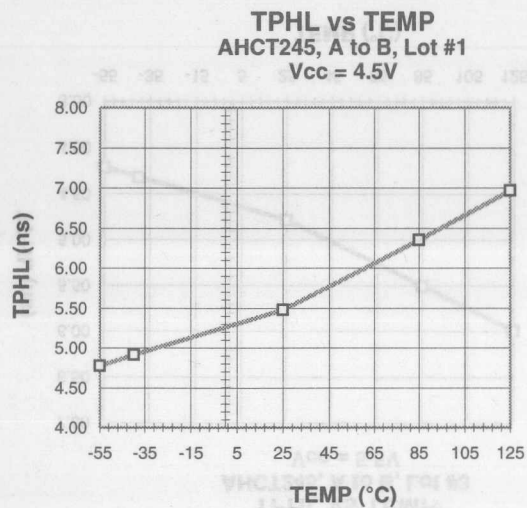
Lot #3

**TPLH vs TEMP**  
AHCT245, A to B, Competitor

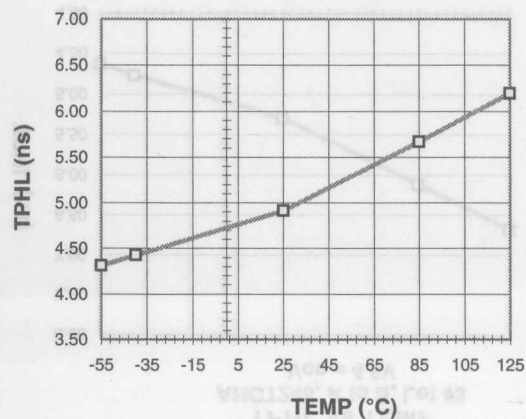
Vcc = 5.5V



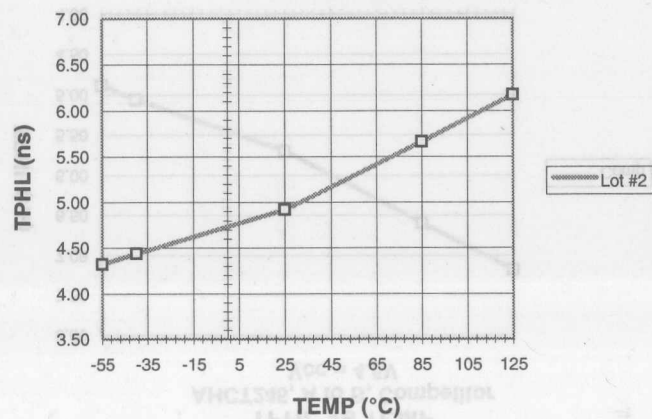
Comp



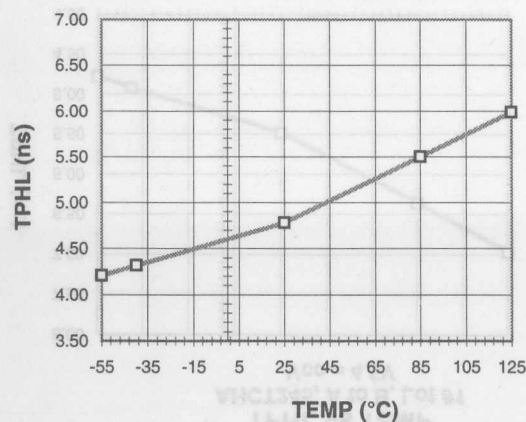
**TPHL vs TEMP**  
AHCT245, A to B, Lot #1  
Vcc = 5.5V



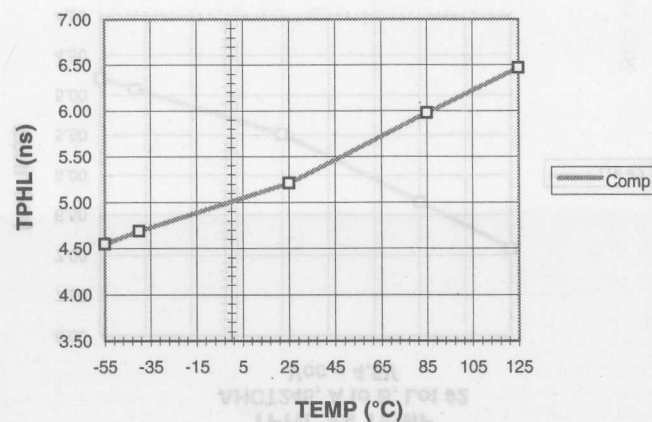
**TPHL vs TEMP**  
AHCT245, A to B, Lot #2  
Vcc = 5.5V

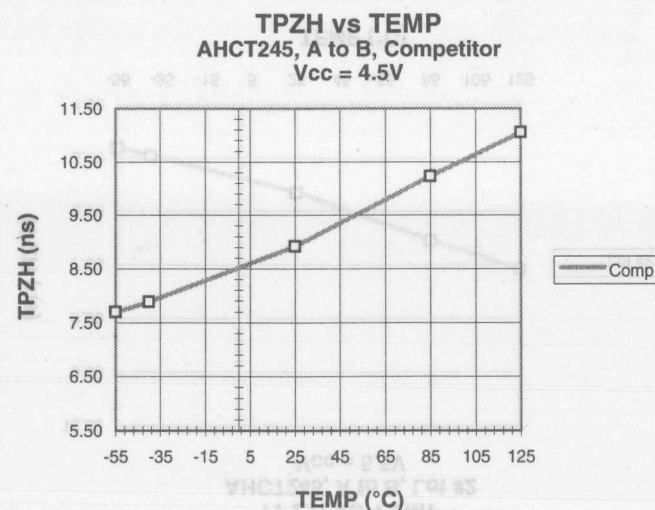
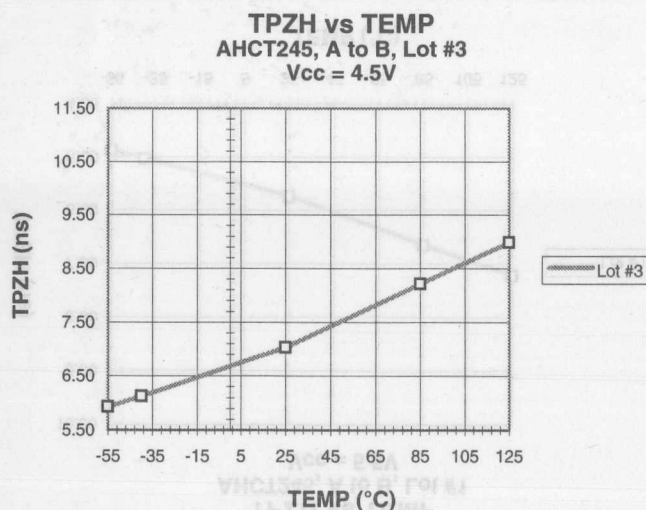
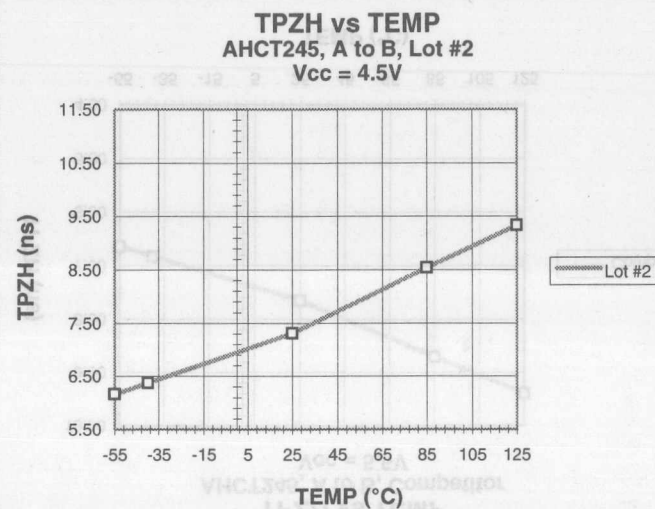
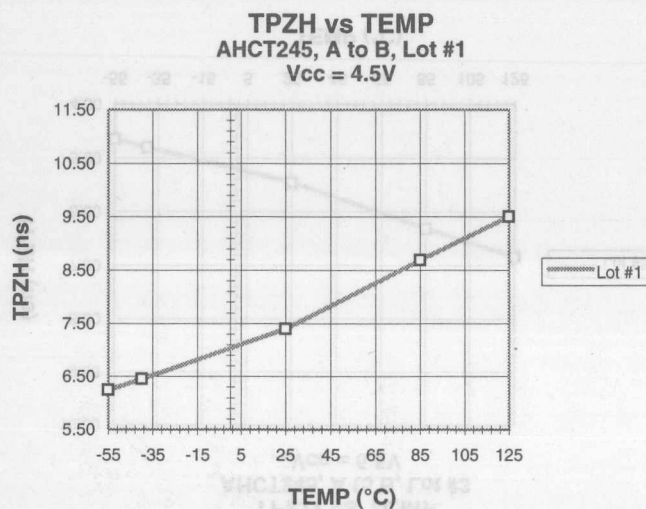


**TPHL vs TEMP**  
AHCT245, A to B, Lot #3  
Vcc = 5.5V

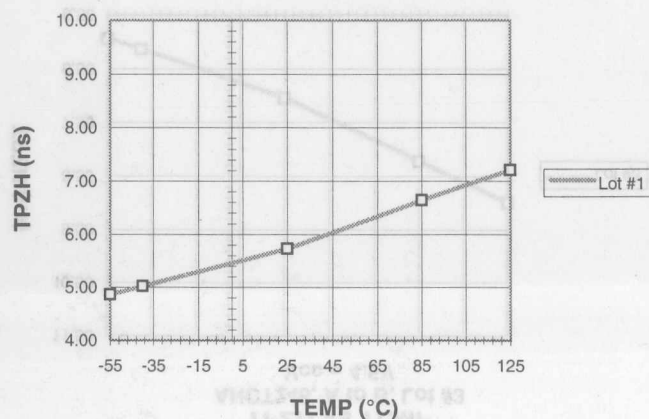


**TPHL vs TEMP**  
AHCT245, A to B, Competitor  
Vcc = 5.5V

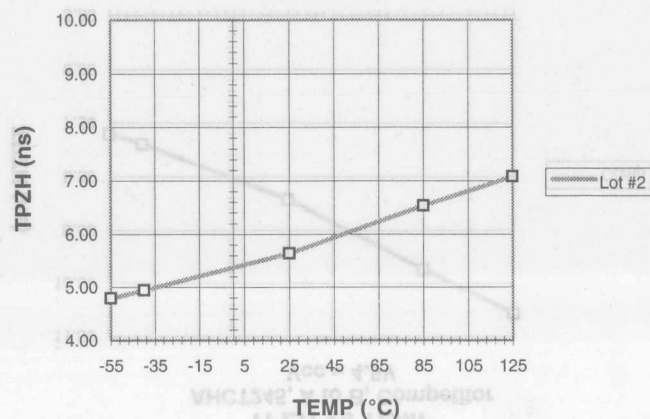




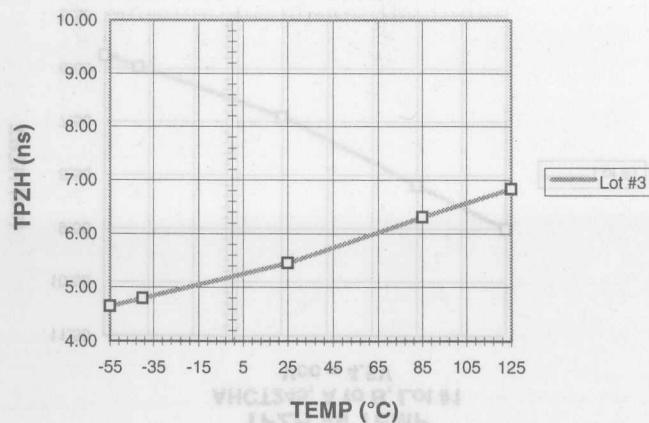
**TPZH vs TEMP**  
AHCT245, A to B, Lot #1  
Vcc = 5.5V



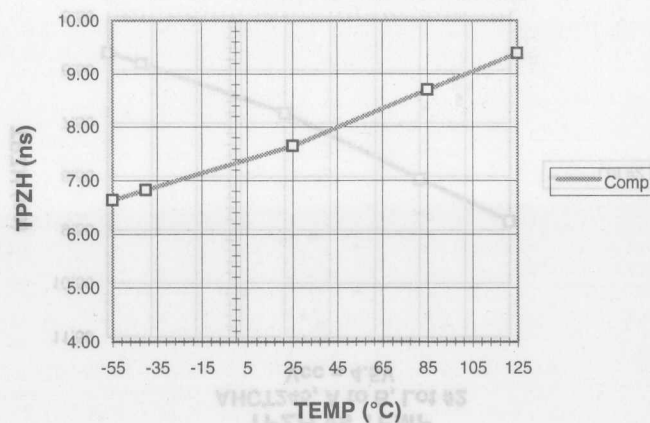
**TPZH vs TEMP**  
AHCT245, A to B, Lot #2  
Vcc = 5.5V



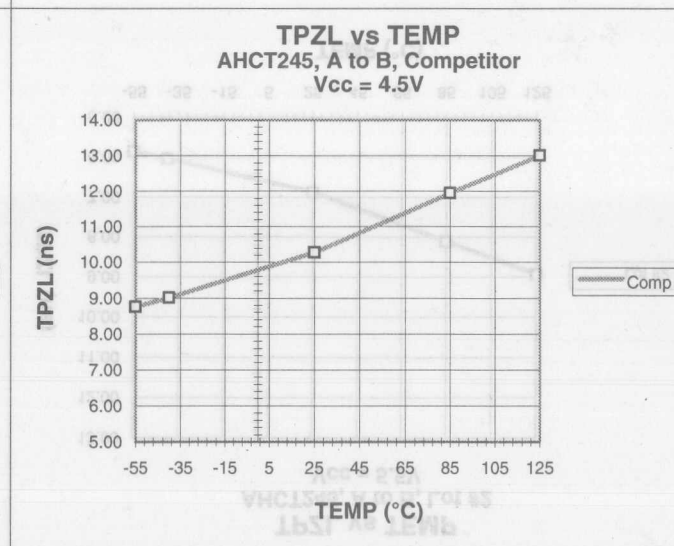
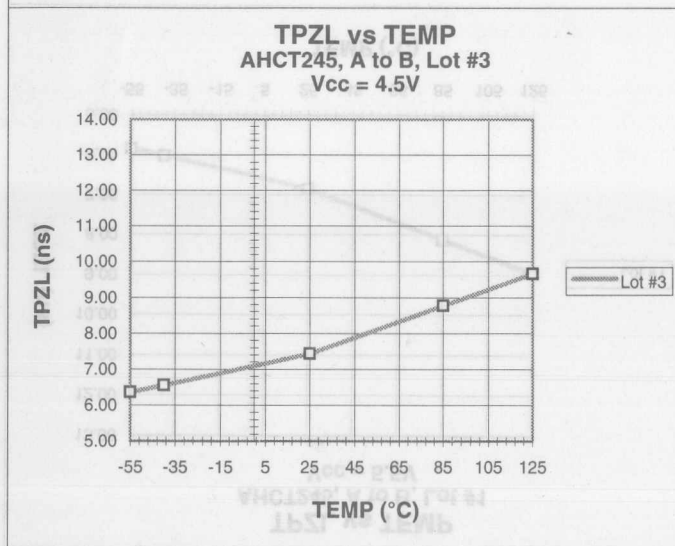
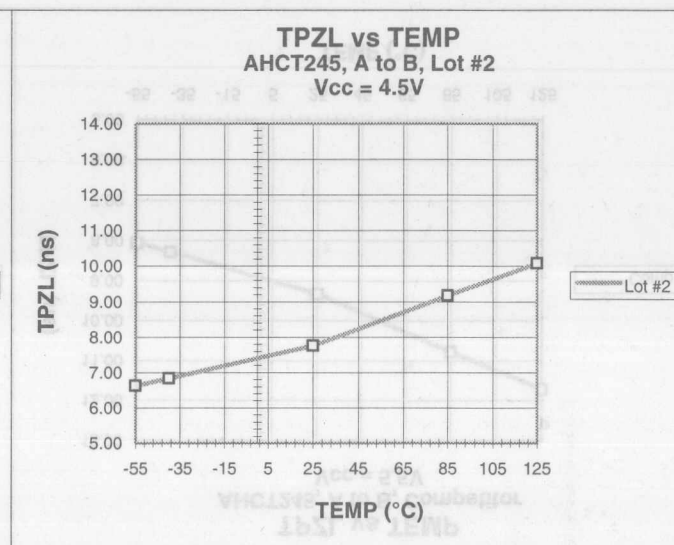
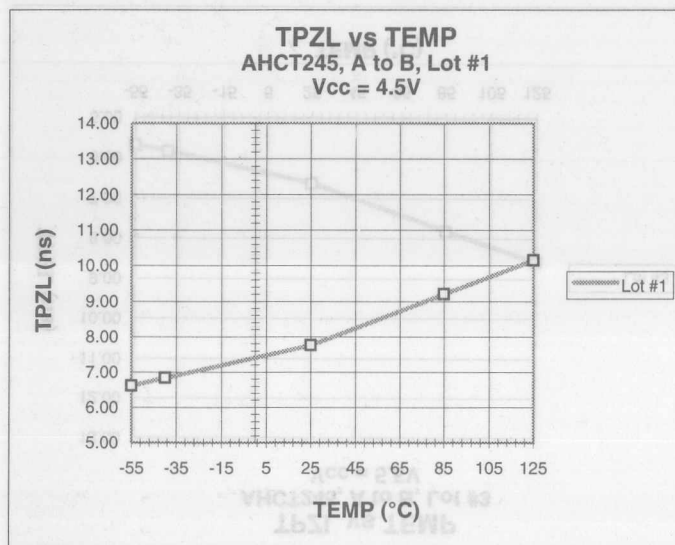
**TPZH vs TEMP**  
AHCT245, A to B, Lot #3  
Vcc = 5.5V



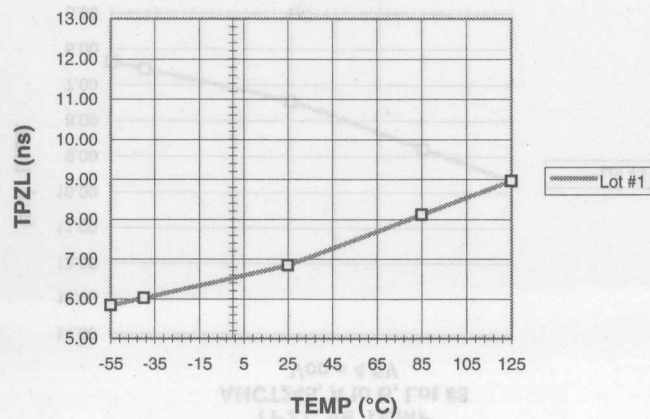
**TPZH vs TEMP**  
AHCT245, A to B, Competitor  
Vcc = 5.5V



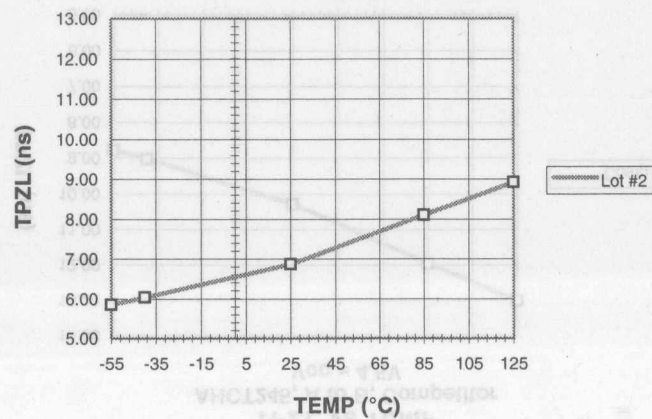




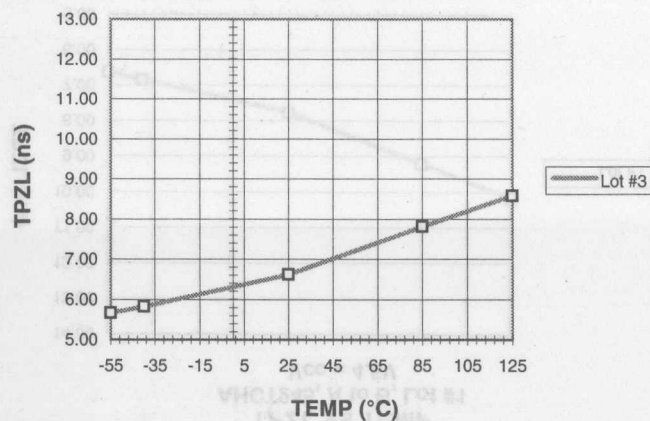
**TPZL vs TEMP**  
AHCT245, A to B, Lot #1  
Vcc = 5.5V



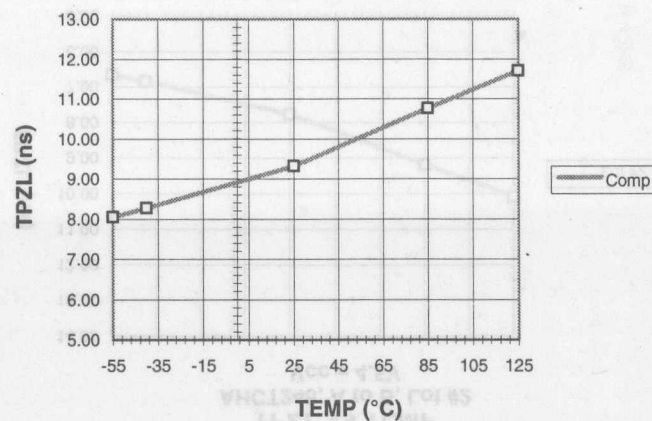
**TPZL vs TEMP**  
AHCT245, A to B, Lot #2  
Vcc = 5.5V

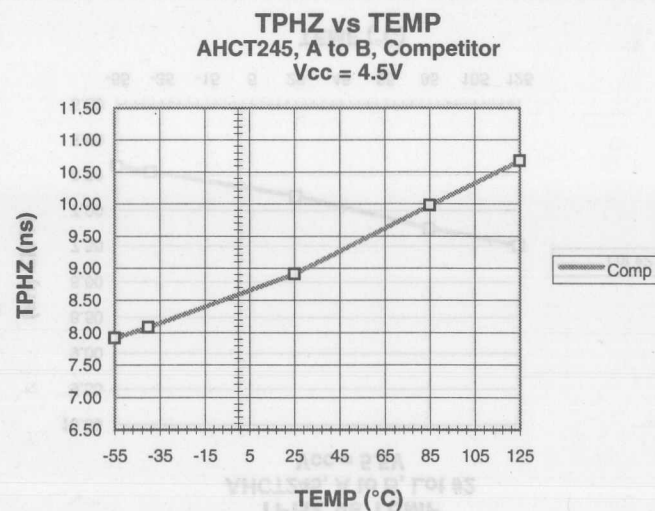
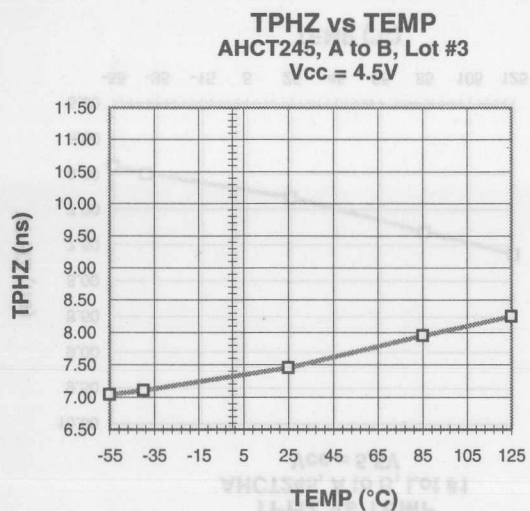
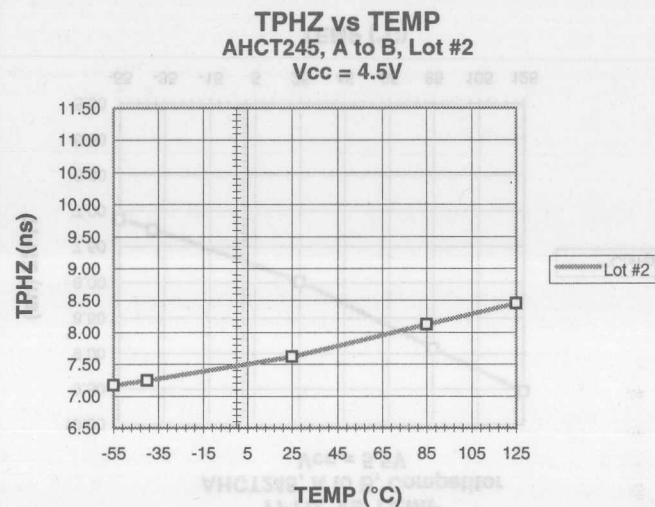
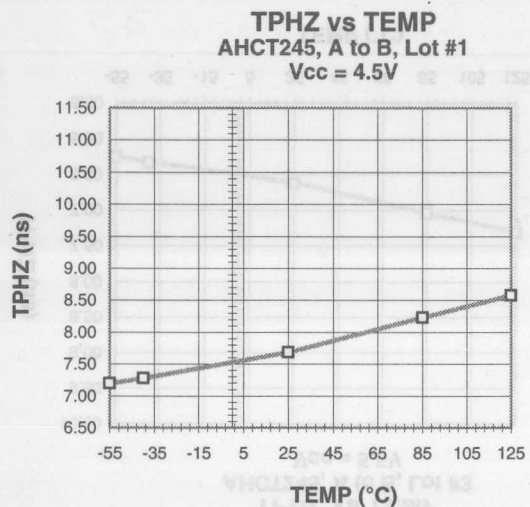


**TPZL vs TEMP**  
AHCT245, A to B, Lot #3  
Vcc = 5.5V

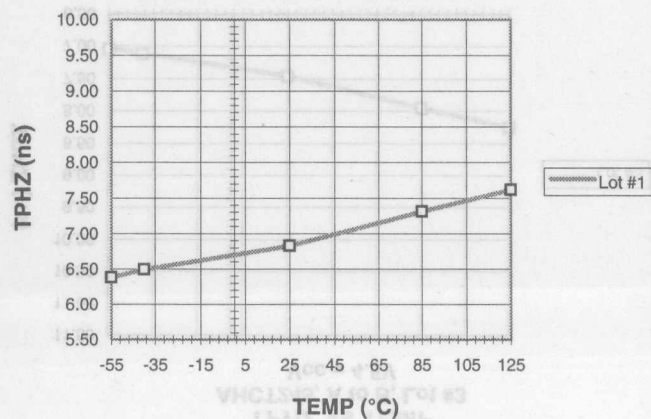


**TPZL vs TEMP**  
AHCT245, A to B, Competitor  
Vcc = 5.5V

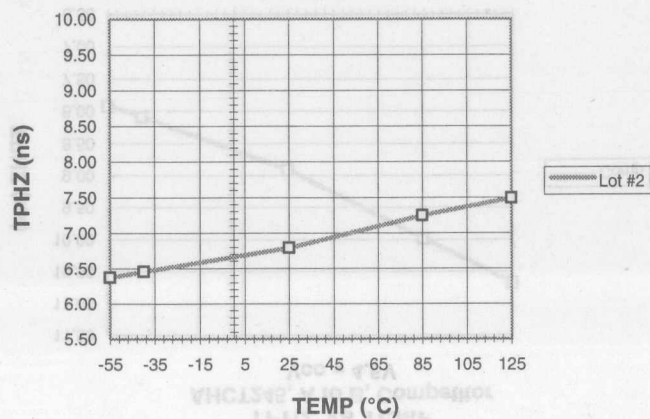




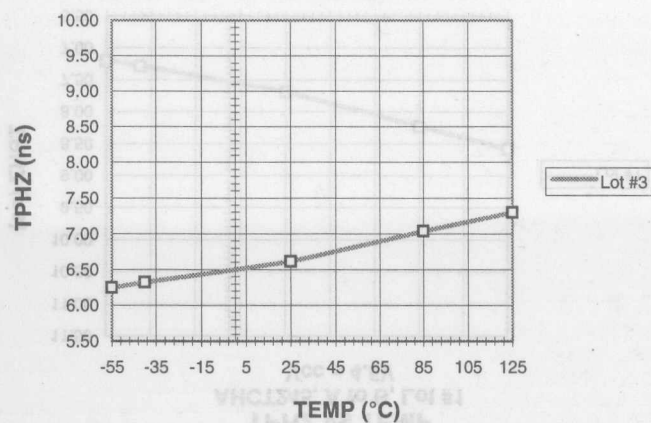
**TPHZ vs TEMP**  
**AHCT245, A to B, Lot #1**  
**V<sub>cc</sub> = 5.5V**



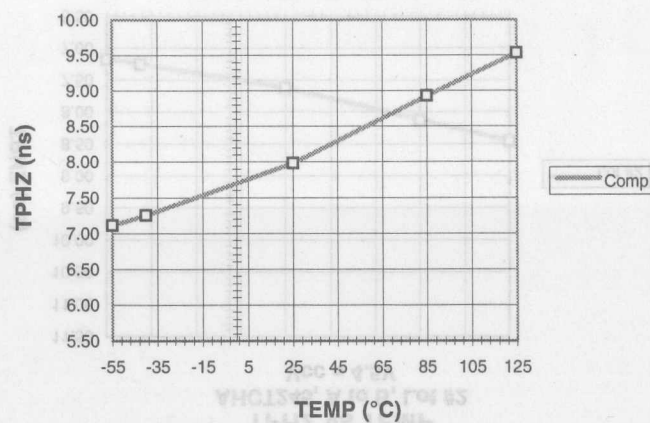
**TPHZ vs TEMP**  
**AHCT245, A to B, Lot #2**  
**V<sub>cc</sub> = 5.5V**

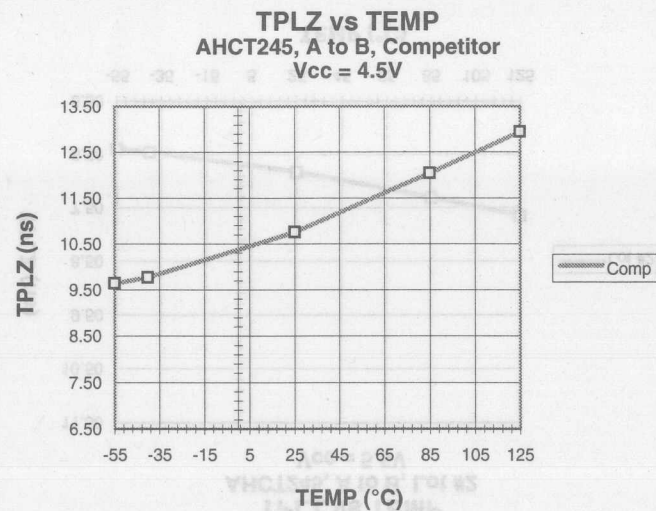
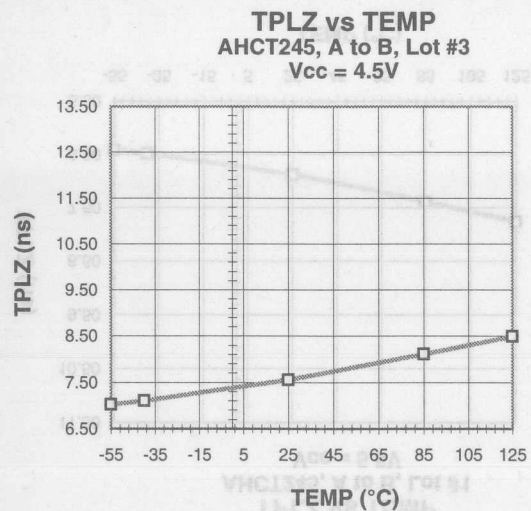
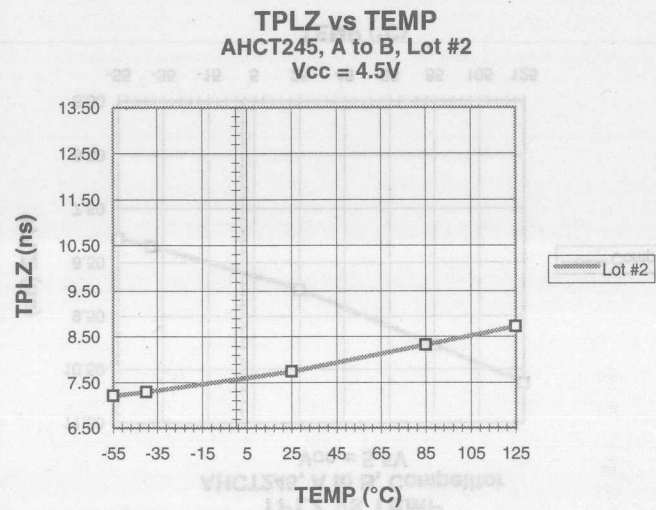
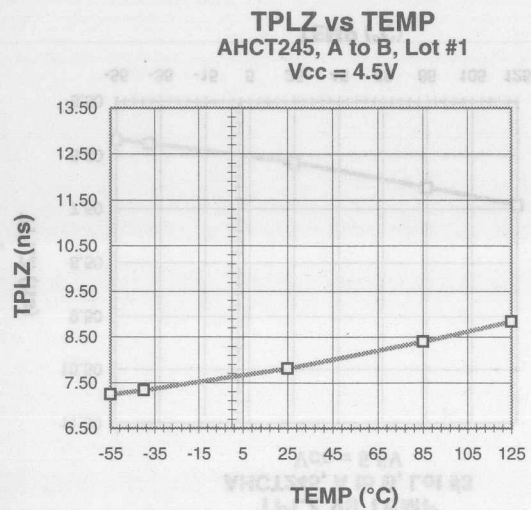


**TPHZ vs TEMP**  
**AHCT245, A to B, Lot #3**  
**V<sub>cc</sub> = 5.5V**



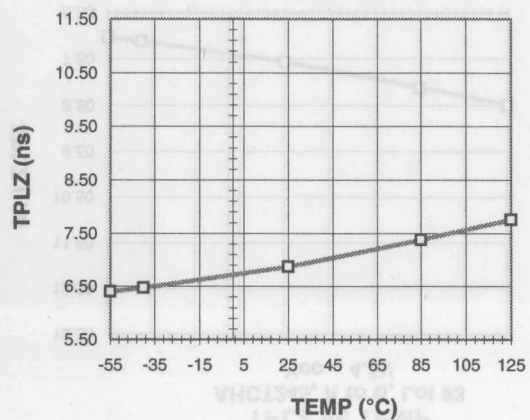
**TPHZ vs TEMP**  
**AHCT245, A to B, Competitor**  
**V<sub>cc</sub> = 5.5V**



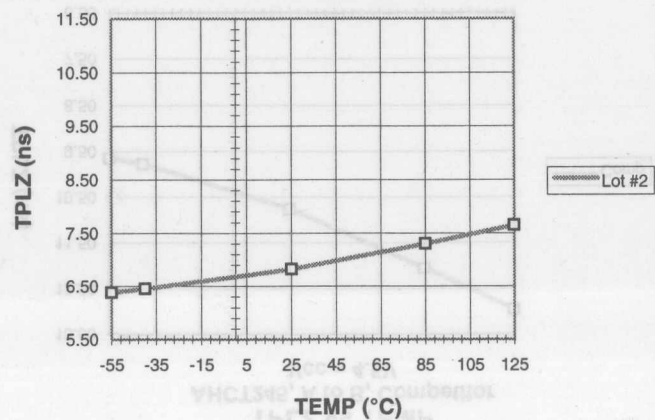




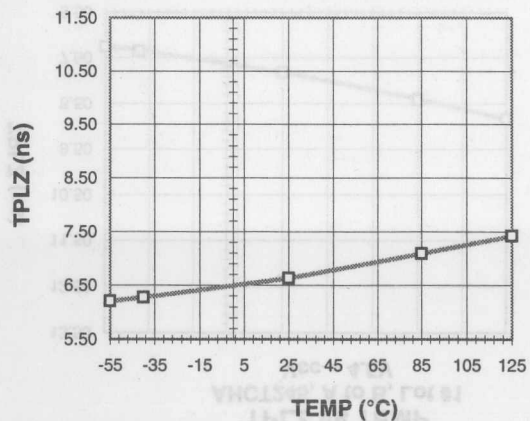
**TPLZ vs TEMP**  
AHCT245, A to B, Lot #1  
Vcc = 5.5V



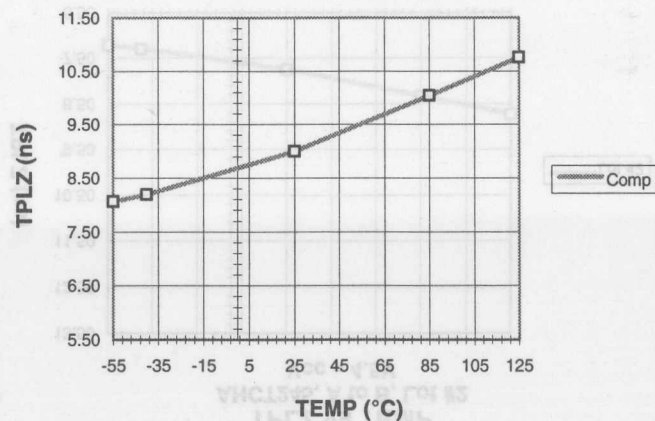
**TPLZ vs TEMP**  
AHCT245, A to B, Lot #2  
Vcc = 5.5V

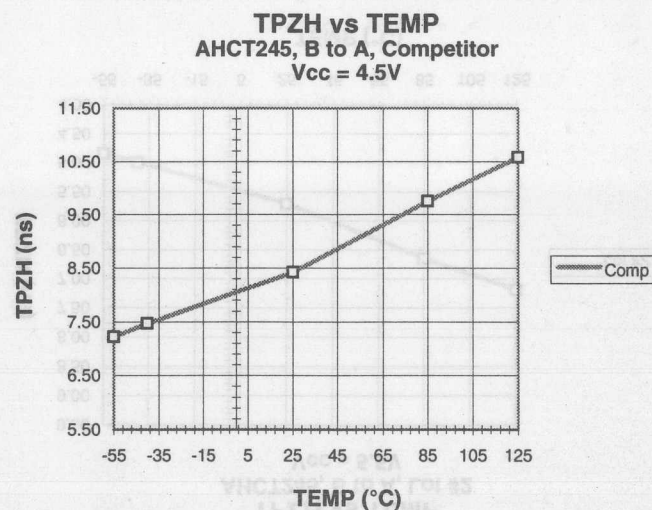
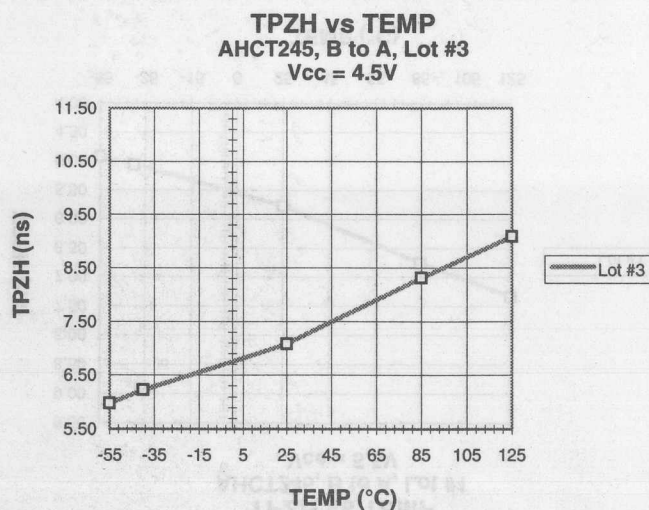
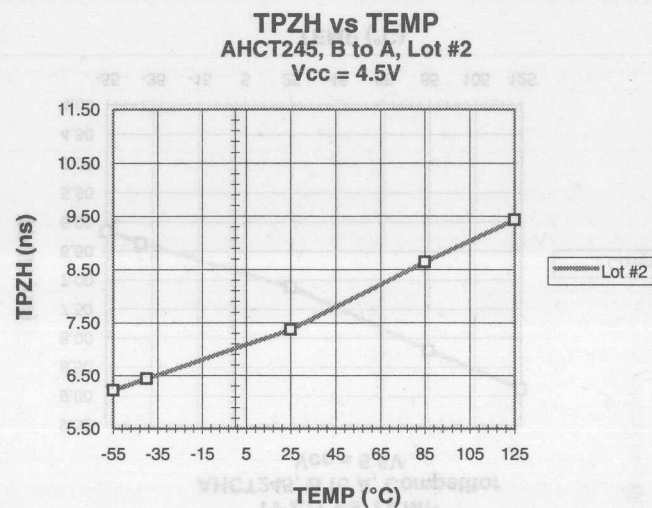
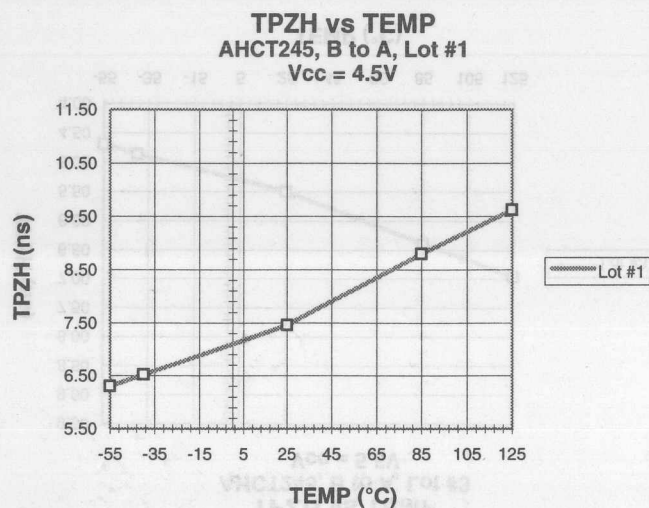


**TPLZ vs TEMP**  
AHCT245, A to B, Lot #3  
Vcc = 5.5V

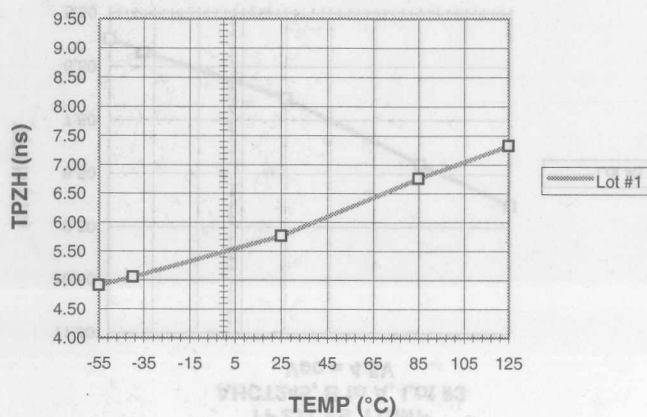


**TPLZ vs TEMP**  
AHCT245, A to B, Competitor  
Vcc = 5.5V

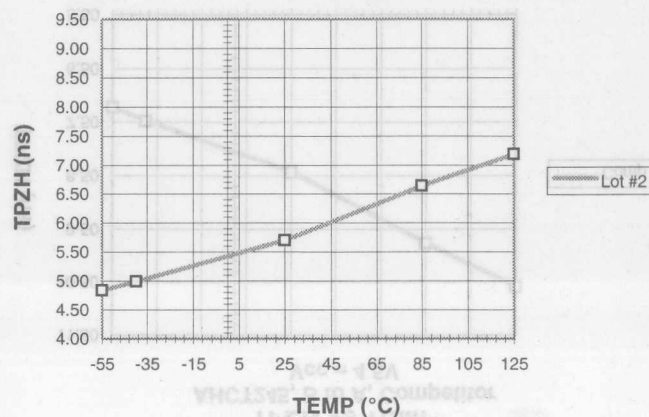




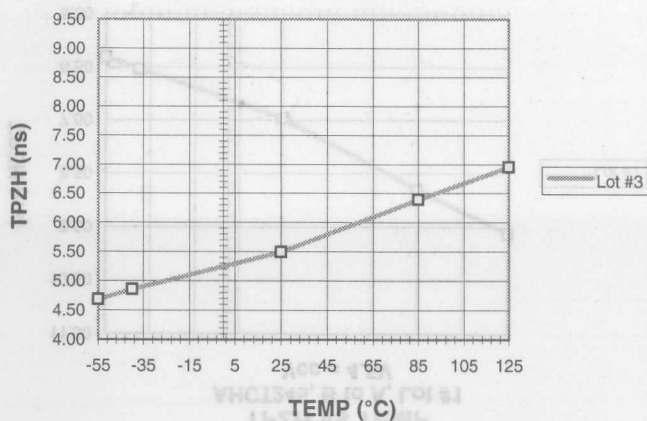
**TPZH vs TEMP**  
**AHCT245, B to A, Lot #1**  
**Vcc = 5.5V**



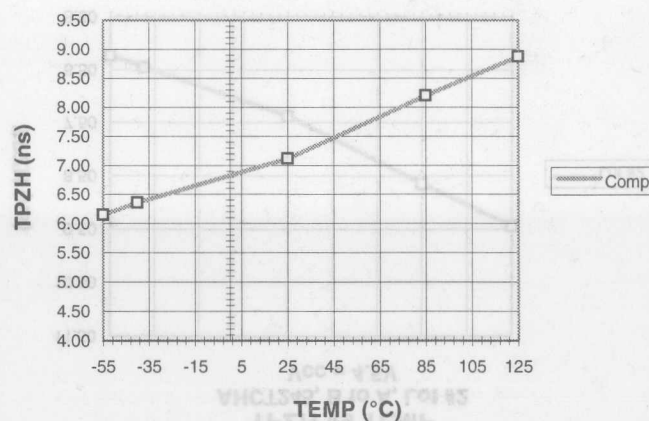
**TPZH vs TEMP**  
**AHCT245, B to A, Lot #2**  
**Vcc = 5.5V**

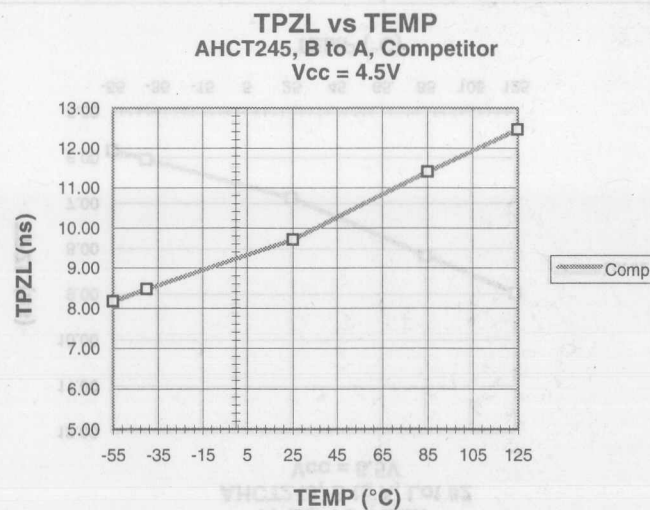
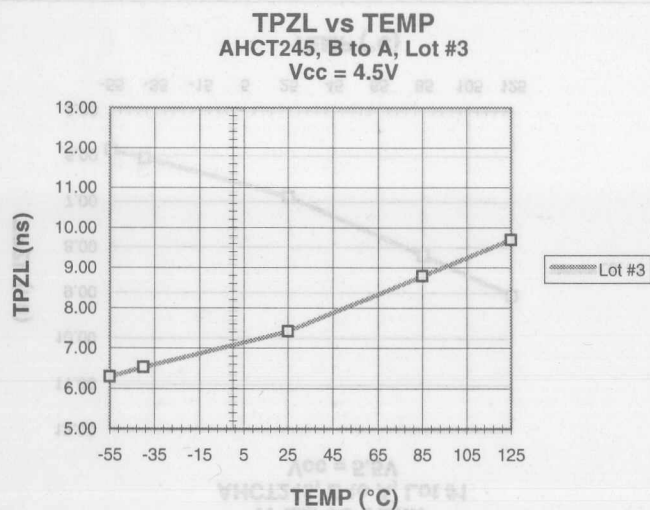
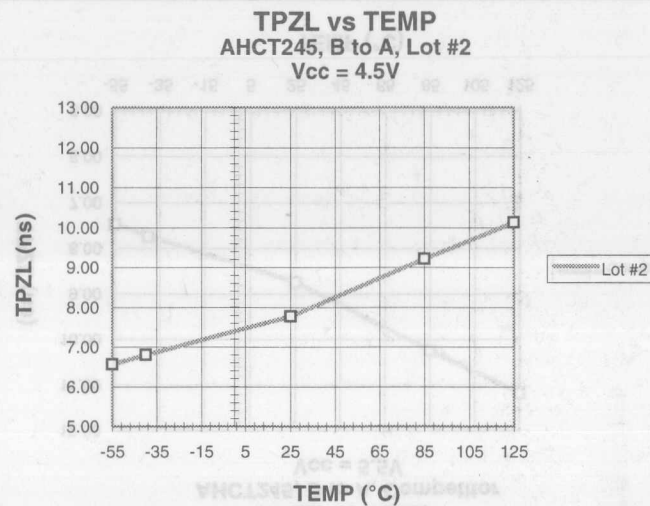
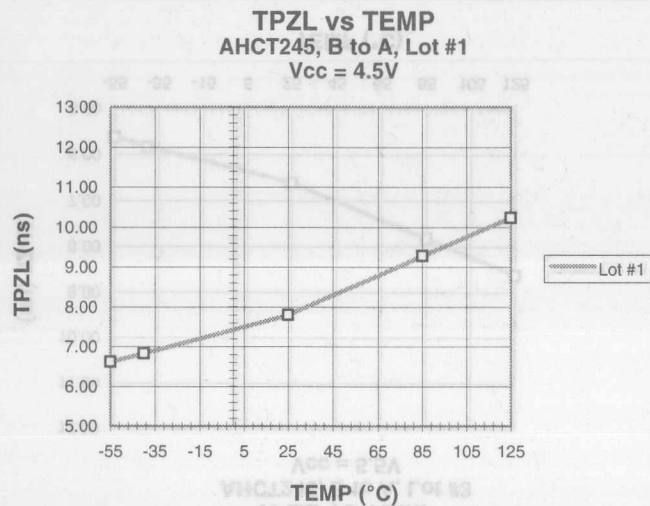


**TPZH vs TEMP**  
**AHCT245, B to A, Lot #3**  
**Vcc = 5.5V**

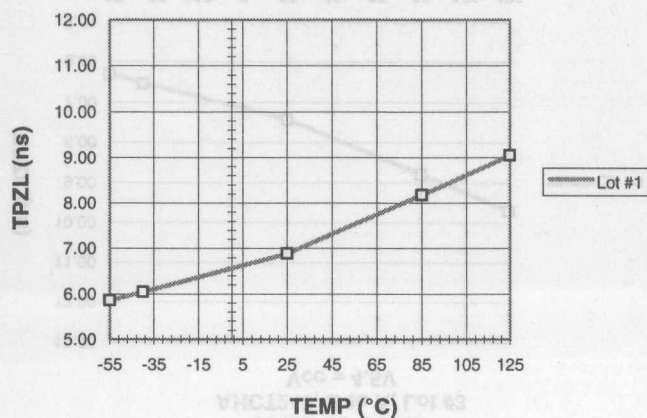


**TPZH vs TEMP**  
**AHCT245, B to A, Competitor**  
**Vcc = 5.5V**

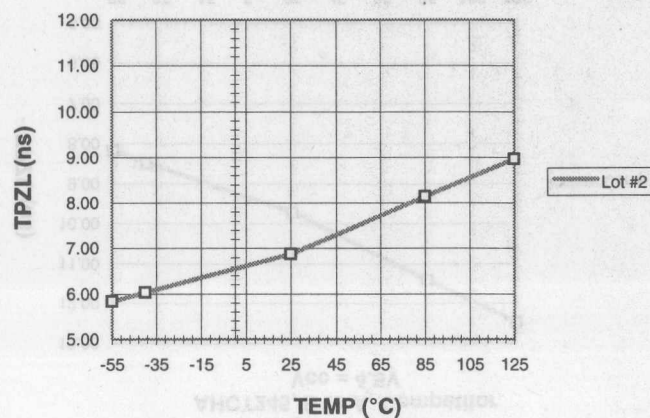




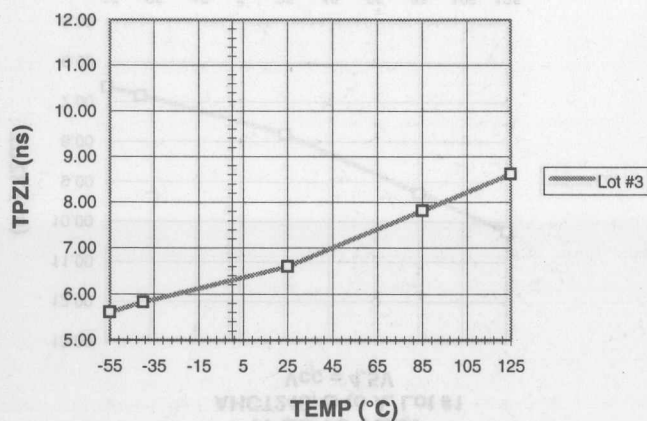
**TPZL vs TEMP**  
AHCT245, B to A, Lot #1  
Vcc = 5.5V



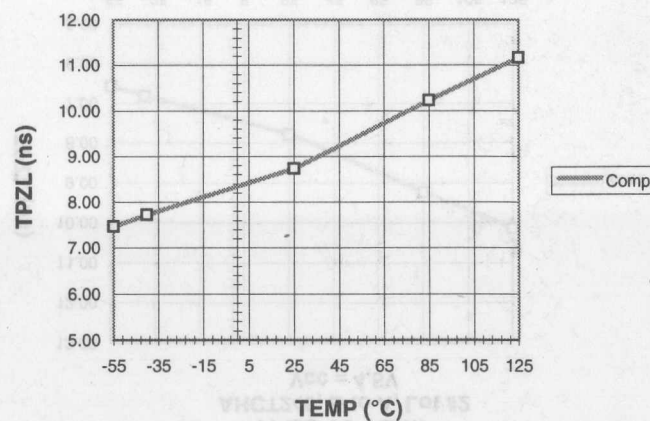
**TPZL vs TEMP**  
AHCT245, B to A, Lot #2  
Vcc = 5.5V



**TPZL vs TEMP**  
AHCT245, B to A, Lot #3  
Vcc = 5.5V

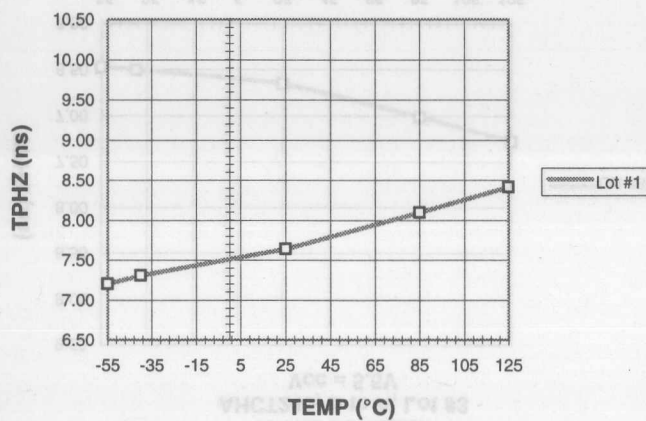


**TPZL vs TEMP**  
AHCT245, B to A, Competitor  
Vcc = 5.5V

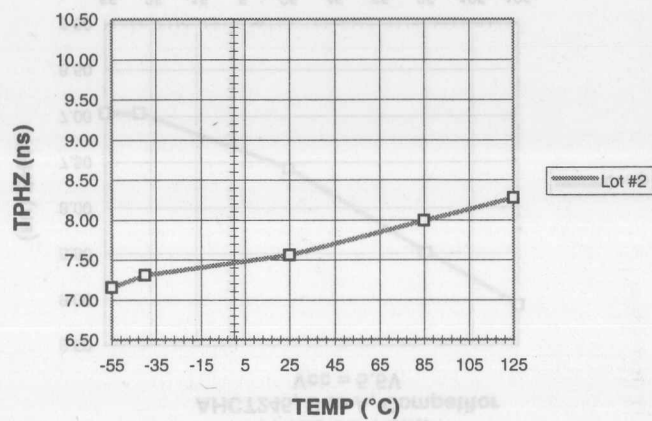




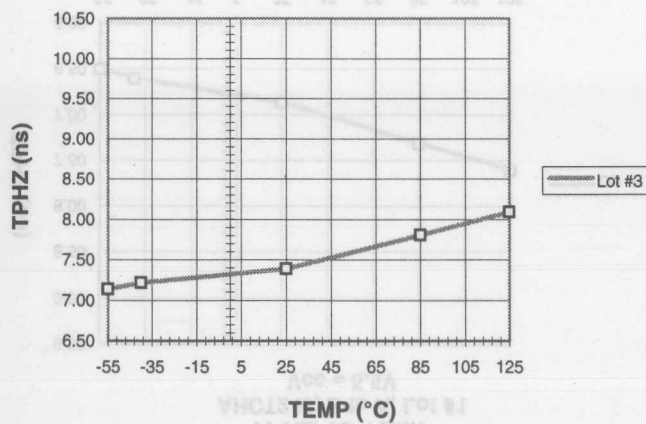
**TPHZ vs TEMP**  
**AHCT245, B to A, Lot #1**  
**V<sub>cc</sub> = 4.5V**



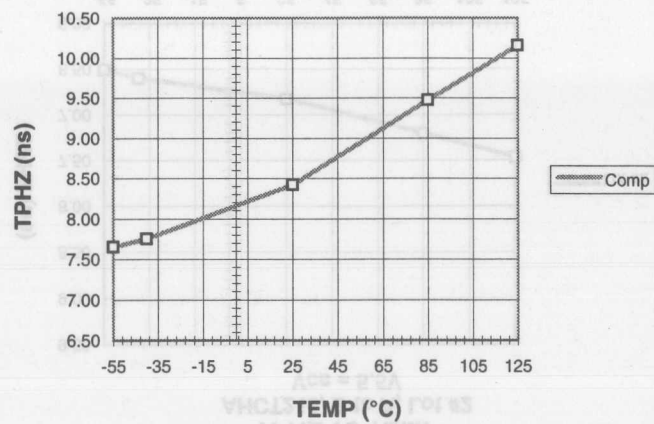
**TPHZ vs TEMP**  
**AHCT245, B to A, Lot #2**  
**V<sub>cc</sub> = 4.5V**



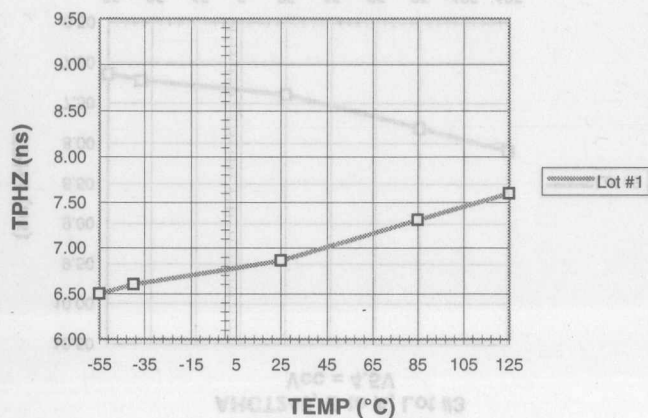
**TPHZ vs TEMP**  
**AHCT245, B to A, Lot #3**  
**V<sub>cc</sub> = 4.5V**



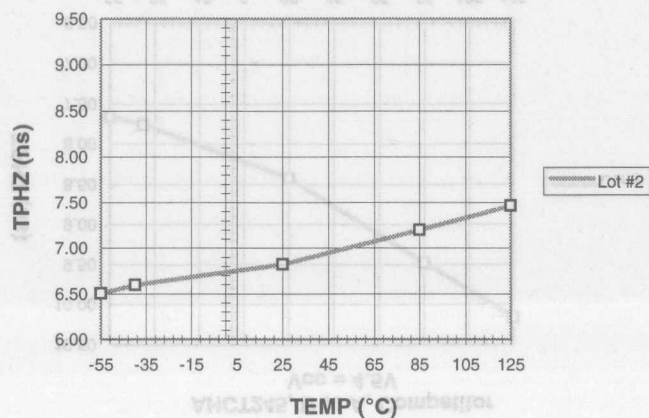
**TPHZ vs TEMP**  
**AHCT245, B to A, Competitor**  
**V<sub>cc</sub> = 4.5V**



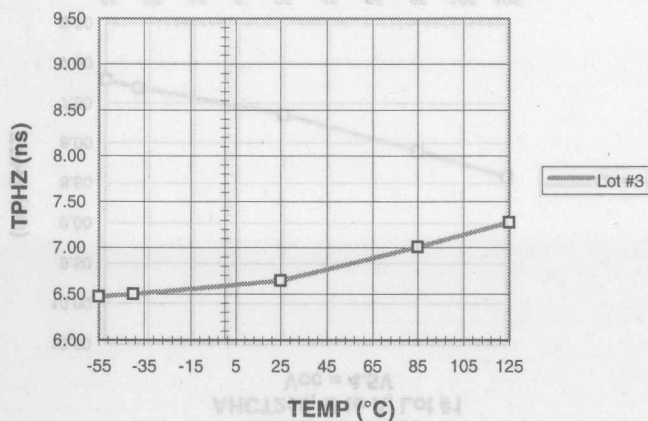
**TPHZ vs TEMP**  
AHCT245, B to A, Lot #1  
Vcc = 5.5V



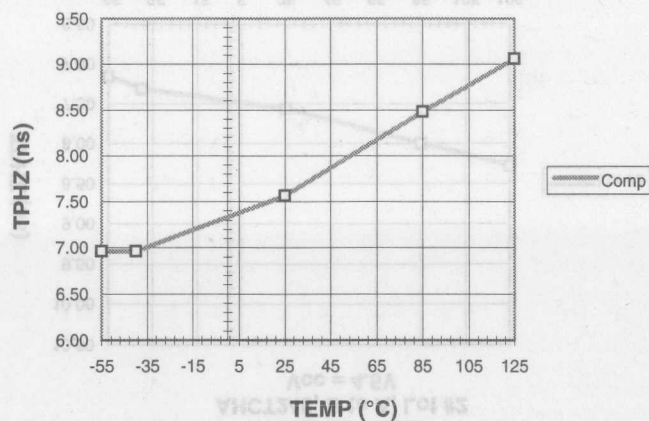
**TPHZ vs TEMP**  
AHCT245, B to A, Lot #2  
Vcc = 5.5V

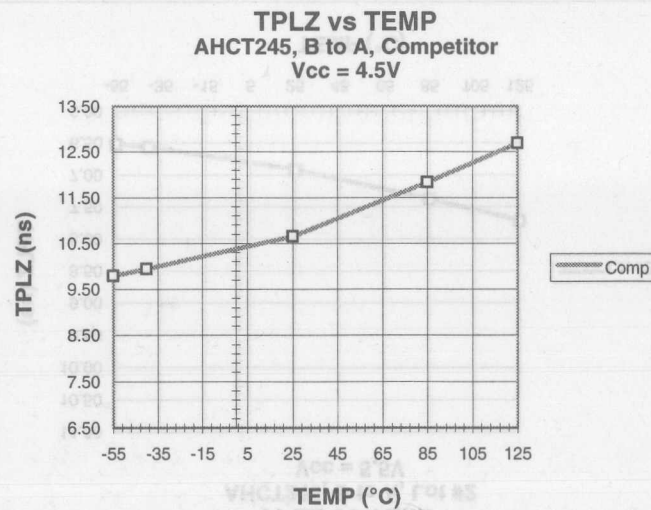
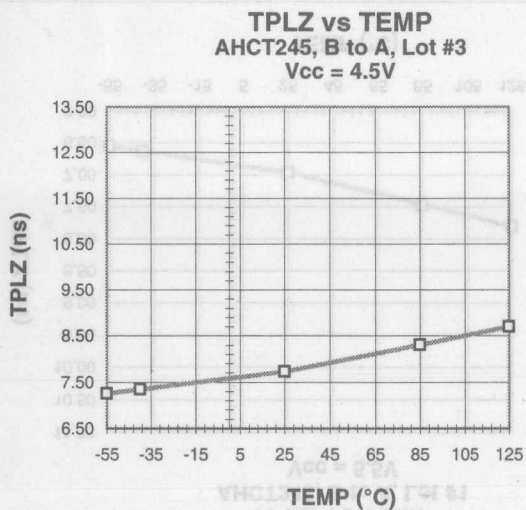
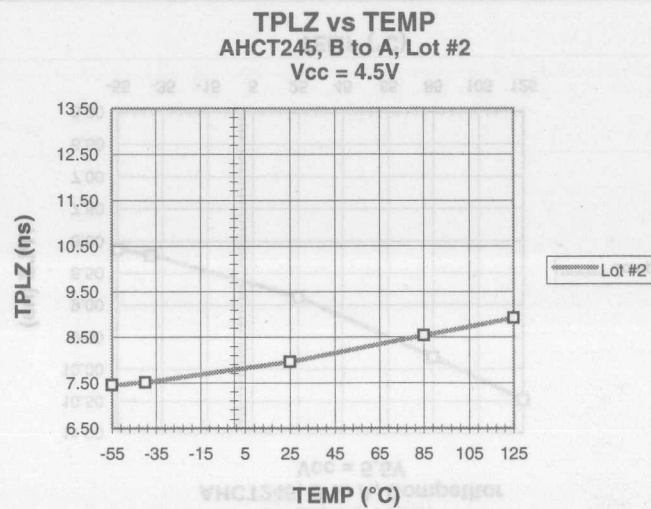
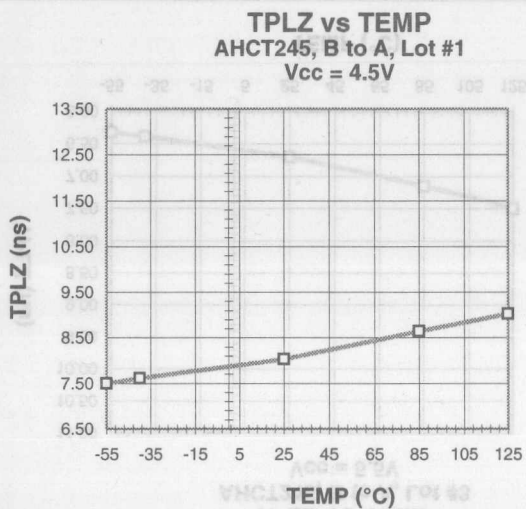


**TPHZ vs TEMP**  
AHCT245, B to A, Lot #3  
Vcc = 5.5V

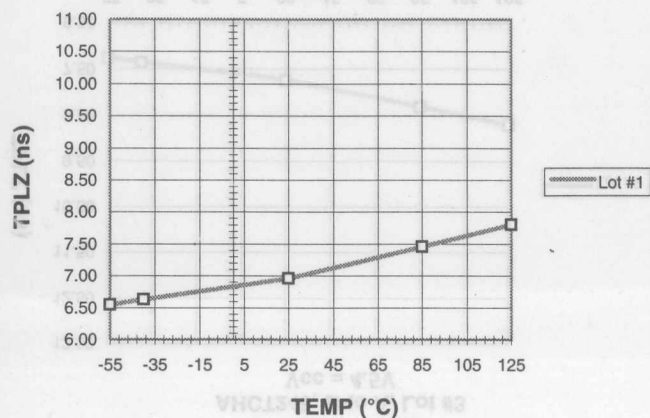


**TPHZ vs TEMP**  
AHCT245, B to A, Competitor  
Vcc = 5.5V

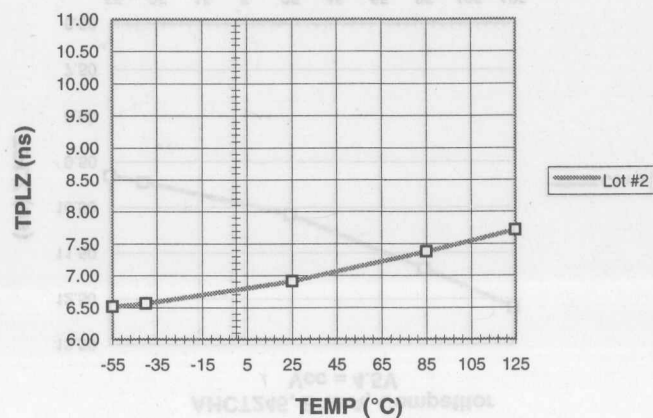




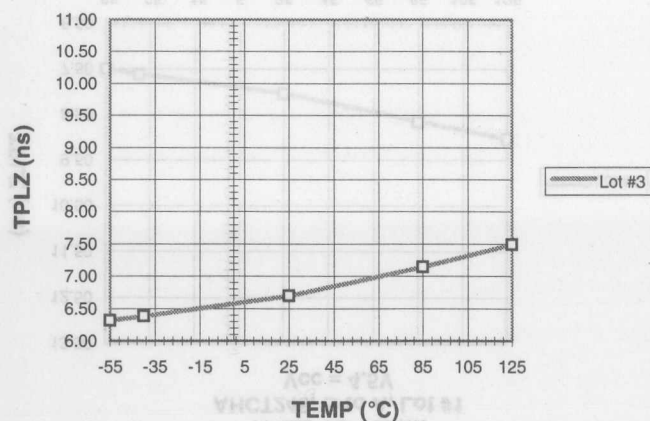
**TPLZ vs TEMP**  
AHCT245, B to A, Lot #1  
Vcc = 5.5V



**TPLZ vs TEMP**  
AHCT245, B to A, Lot #2  
Vcc = 5.5V



**TPLZ vs TEMP**  
AHCT245, B to A, Lot #3  
Vcc = 5.5V



**TPLZ vs TEMP**  
AHCT245, B to A, Competitor  
Vcc = 5.5V

